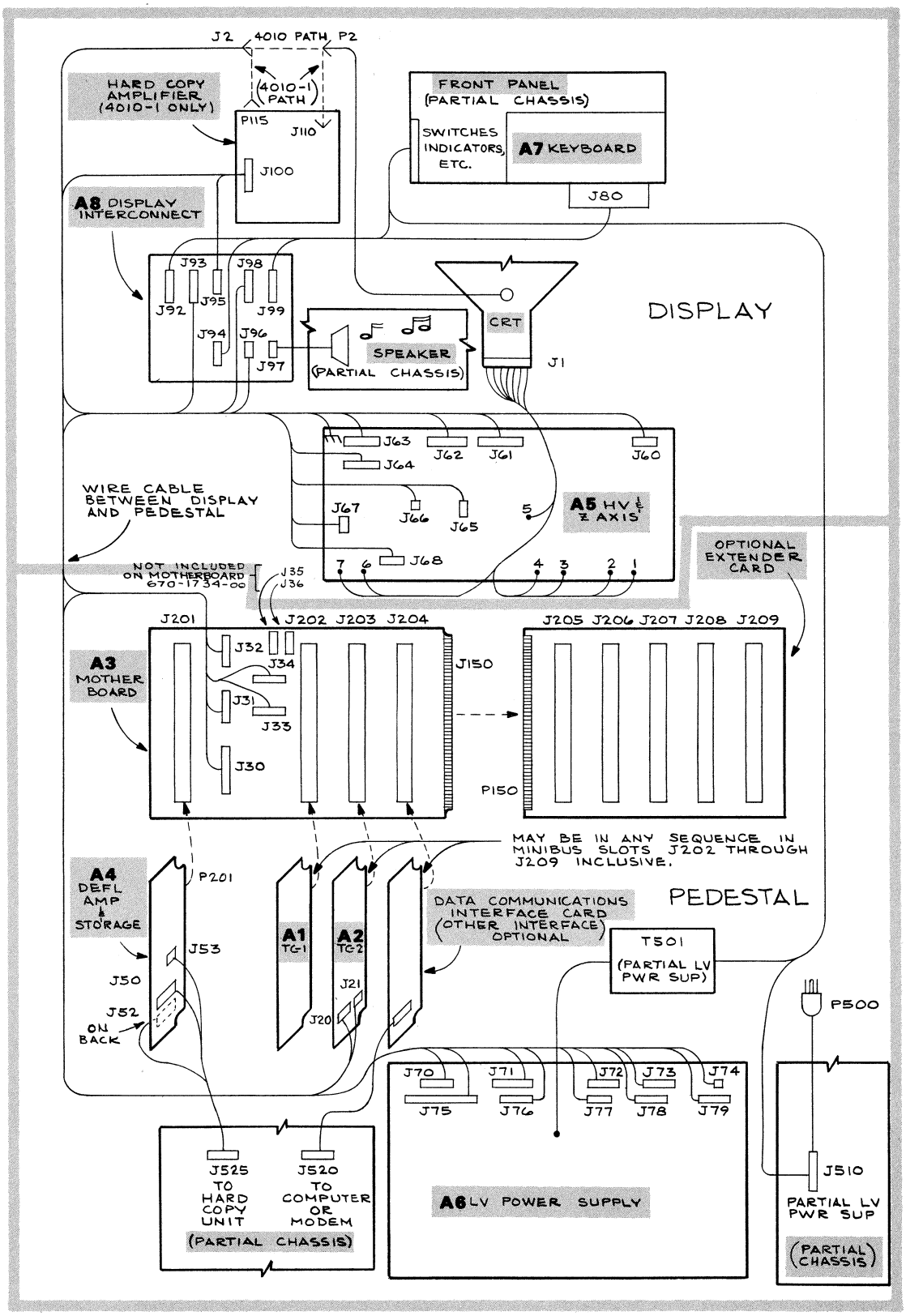
CIRCUIT DESCRIPTION

CONTENTS


J2
4010 PATH
P2
HARD COPY AMPLIFIER (4010-1 ONLY)
(4010-1 PATH)
P115
J110
J100
FRONT PANEL (PARTIAL CHASSIS)
SWITCHES INDICATORS, ETC.
A7 KEYBOARD
J80
A8 DISPLAY INTERCONNECT
J93
J98
J92
J95
J99
J94
J96
J97
SPEAKER (PARTIAL CHASSIS)
CRT
J1
DISPLAY
J63
J64
J62
J61
J60
WIRE CABLE BETWEEN DISPLAY AND PEDESTAL
J67
J66
J65
5
A5 HV & Z AXIS
7
6
J68
4
3
2
1
NOT INCLUDED ON MOTHERBOARD 670-1734-00
J35
J36
OPTIONAL EXTENDER CARD
J201
J202 J203 J204
J205 J206 J207 J208 J209
A3 MOTHER BOARD
J32
J34
J31
J33
J30
J150
P150
MAY BE IN ANY SEQUENCE IN MINIBUS SLOTS J202 THROUGH J209 INCLUSIVE.
A4 DEFL AMP & STORAGE
P201
J53
J50
J52 ON BACK
A1 TG-1
A2 TG-2
J21
J20
DATA COMMUNICATIONS INTERFACE CARD (OTHER INTERFACE) OPTIONAL
PEDESTAL
T501 (PARTIAL LV PWR SUP)
P500
J70
J71
J72
J73
J74
J75
J76
J77
J78
J79
J525 TO HARD COPY UNIT
J520 TO COMPUTER OR MODEM
(PARTIAL CHASSIS)
A6 LV POWER SUPPLY
J510
PARTIAL LV PWR SUP
(PARTIAL CHASSIS)

@

GENERAL INFORMATION

Introduction

The description of Terminal concepts and circuit operation is separate from the block diagrams and circuit schematics. This allows the reader to have the diagram available while reading the text. When troubleshooting, select the proper schematic diagram for the board number installed in your instrument. Assembly numbers (Ax) on the schematic diagrams and the board numbers (670-0000-00) are a guide to the parts listing for the board in the Electrical Parts List. Assembly numbers are also given on the Connector and Wiring Diagram Fig. 6-1.

This section also contains a Wire List, and a Dictionary of Line Titles that will prove beneficial in understanding logic flow on the Interconnection Mother Board (minibus). A Wire List Explanation shows how to use the Wire List in conjunction with the Connectors and Wiring Diagram (Fig. 6-1) and the Interconnecting Mother Board diagrams. The Dictionary of Line Titles should be read before any of the block diagram or circuit descriptions. The Wire List Explanation should be read before attempting to trace signals between schematics.

Diagrams and Circuit Description Information

The circuit descriptions with the block diagrams and schematics will allow those not familiar with 4010 operation to progress from a basic understanding to a fairly detailed understanding of 4010 concepts and operation. It is recommended that those unfamiliar with 4010 operation read the following block diagrams and their respective descriptions in the following order.

1. Terminal/Computer Communication Concepts. This block diagram (on DATA FLOW tab) with its description will acquaint you with the basics of Terminal/computer operation. It will also introduce for the first time the basic electrical sections of the Terminal, namely, Keyboard, Terminal Control Logic and the Display Unit.

2. Terminal Data Flow Block Diagram and Description. This block acquaints you with the basic data flow within the 4010. It shows the tie-in of the major electrical components for the Alphanumeric Mode, the Graphic Plot Mode, and the Graphic Input Mode.

3. Alphanumeric Block Mode Diagram and Description. This block shows the operation and logic tie-in of TC-1 and TC-2 in the Alpha Mode.

4. Graphic Modes Block Diagram and Description. This block provides the logic tie-in of TC-1 and TC-2, for Graphic Plot and Graphic Input Mode operation.

5. Display Unit Block Diagram and Description. This block diagram and description gives a basic understanding of the circuitry associated with the Display Unit.

The above block diagrams and associated descriptions will, in most cases, aid in isolating a problem to a specific circuit card. Should you desire to further isolate the problem they will provide you with enough information as to where to go next.

DICTIONARY OF LINE TITLES

General

The following is a description of interconnecting (minibus) signals and the explanation of their purpose and operation. Signals are shown in their active states. Those with bars indicate that the source must pull the signal line low to be active. Those without bars indicate that the source must pull the signal line high to be active.

$\overline{\text{BIT 1}}$–$\overline{\text{BIT 8}}$	Data to and from the Terminal/computer.
$\overline{\text{SEND}}$	Indicates data is to be sent as a full 8-bit byte (do not add parity).
$\overline{\text{CPUNT}}$	Means data is about to be sent to the minibus by the computer (Interface). Must be sent at least 5 microseconds before data is placed on $\overline{\text{BIT1-8}}$ lines and must remain low until after the trailing edge of the strobe(s) associated with the transfer.

$\overline{\text{TSTROBE}}$ — Strobes data into the Terminal to be displayed on the screen, etc. 1.6 microsecond pulse synchronized to the 614 kHz clock.

$\overline{\text{CSTROBE}}$ — Strobes data to the computer. Pulse width 1.6 microseconds sync'd to the clock. Must not occur more than 2 microseconds after $\overline{\text{CPUNT}}$ goes low. $\overline{\text{TSTROBE}}$ may be asserted simultaneously (from the same source) to provide local copy to the Terminal.

$\overline{\text{TBUSY}}$ — Terminal is busy writing a character or vector, etc. $\overline{\text{TBUSY}}$ controls the timing of data transmitted to the Terminal. Upon receipt of a byte of data, the Terminal will assert $\overline{\text{TBUSY}}$ by the trailing edge of $\overline{\text{TSTROBE}}$ if the byte is to make the Terminal busy. No condition, with the exception of MARG, shall assert $\overline{\text{TBUSY}}$ except momentarily. (MARG can be patched out of $\overline{\text{TBUSY}}$.) The Terminal will, however, accept data if $\overline{\text{TBUSY}}$ is high or low although the results in that case are not defined. $\overline{\text{TBUSY}}$ does not inhibit transmission of data from the Keyboard to the computer.

$\overline{\text{CBUSY}}$ — Computer (Interface) is busy accepting a character. Controls the timing of coordinate data transmitted to the computer. A low on $\overline{\text{CBUSY}}$ will not inhibit the Keyboard, allowing Keyboard interrupts when $\overline{\text{CPUNT}}$ is not asserted. Interfaces which must lock out the Keyboard should do so with $\overline{\text{KLOCK}}$.

$\overline{\text{TSUP}}$ — Suppresses Terminal response to $\overline{\text{TSTROBE}}$. $\overline{\text{TSUP}}$ should be used by auxiliary devices which need to blank the Terminal to incoming data, such as a paper tape punch when punching binary data. $\overline{\text{BTSUP}}$ should be asserted in response to $\overline{\text{CPUNT}}$ by devices (such as buffers used in error correction schemes) intended to intercept data on behalf of the Terminal. In such cases the assertion of $\overline{\text{BTSUP}}$ should be delayed 2 clock periods to avoid interference with copy of locally generated data.

$\overline{\text{BTSUP}}$ — Blanks the entire Terminal (including aux devices to data). A typical use is in a multi-drop system to suppress messages to other terminals. If the Keyboard is to be active while the Terminal is blanked to incoming data, $\overline{\text{BTSUP}}$ should be asserted only in response to $\overline{\text{CPUNT}}$, delayed two clock cycles from the beginning of $\overline{\text{CPUNT}}$.

LCE — Indicates last character sent to Terminal was the ESC (Escape) control character.

$\overline{\text{CSUP}}$ — Inhibits the Interface from accepting $\overline{\text{CSTROBE}}$. This signal is used by devices such as line buffers which need to intercept data destined for the computer.

$\overline{\text{KLOCK}}$ — Inhibits Keyboard. Normally held at a high level.

$\overline{\text{TAPEFETCH}}$ — A pulse or level provided by (typically) some small computer interface to cause a paper tape reader or analagous device to read data.

$\overline{\text{Z}}$ — Z axis information.

$\overline{\text{UP}}$, $\overline{\text{DOWN}}$, $\overline{\text{LEFT}}$, $\overline{\text{RIGHT}}$ — Counting pulses for X and Y Registers.

MARG — Indicates that the Terminal is at Margin 1. With a directly connected Interface this corresponds to Page Full. High active.

$\overline{\text{EOL}}$ — Indicates that the X Register is counting past the right margin (end of line). Used by the Automatic Carriage Return/Line Feed logic. When in the Alpha Mode, $\overline{\text{EOL}}$ going active causes an Automatic Carriage Return (CR)/Line Feed (LF) function.

$\overline{\text{TOPEN}}$ — Disables Top-of-Page circuit allowing an increased number of lines. Not brought out to minibus except by straps. Activation of $\overline{\text{TOPEN}}$ depends upon user requirements.

$\overline{\text{HOME}}$ — Master reset for all logic. Origin in Keyboard (Reset key) and TC-1 when power is initialized.

$\overline{\text{HIY}}$, $\overline{\text{LOY}}$, $\overline{\text{HIX}}$, $\overline{\text{LOXE}}$ — Used to load data into the Y or X Data Latches and (LOXE) to draw vectors.

$\overline{\text{GRAF}}$ — Originates in TC-1. Asserting a low on $\overline{\text{GRAF}}$ will set Graphic Plot Mode.

$\overline{\text{NOLI}}$ — Suppresses Linear Interpolation vector drawing and timing circuitry on TC-1 and TC-2. Asserted by TC-1 when in Alpha Mode.

$\overline{\text{DRBUSY}}$ — If not during an ERASE cycle:

Asserted by the Hard Copy Unit to set up the display for hard copy readout.

$\overline{\text{DRBUSY}}$ should be asserted before the trailing edge of $\overline{\text{MAKE COPY}}$ in order to hold the Terminal in BUSY during the scan.

If during an ERASE cycle:

Asserted by the display for the duration of the erase cycle, during which information may not be written on the screen.

$\overline{\text{HCU}}$ — Indicates that the Hard Copy Unit is capable of accepting a $\overline{\text{MAKE COPY}}$ request.

$\overline{\text{AUXSENSE}}$ — Status bit line reserved for auxiliary device(s). Note that $\overline{\text{HCU}}$ may also be used by aux device(s) if no Hard Copy Unit is connected and powered up. Disables Graphic Lookahead. (Graphic Lookahead is the ability of TC-1 and TC-2 to pre-load the Graphic data bytes, HIY, LOY, and HIX while the current vector is being drawn. Receipt of the LOXE Byte is delayed until the current vector drawing is completed.)

$\overline{\text{GIN}}$ — When originating in TC-2, indicates that the cross-hair cursor is on or that coordinate information is being transmitted to the computer. Disables the Alpha Cursor, Top of Page, Margin Shifter, and CR/LF circuits. Sets Echoplex Suppression. Asserted by TC-1 or options when entering Graphic Plot Mode in order to insure that the Character Generator is disabled.

$\overline{\text{FPAUSE}}$ — Indicates that the X Register has folded over in the process of normal counting. Will go active with CR, FF, ETB (control characters), or RESET ($\overline{\text{HOME}}$ signal). Used to generate the pause required for proper operation of the Auto Linefeed circuit when used with a clocked interface. (Also used internally on TC-2 in Graphic Input Mode.)

$\overline{\text{ECHO}}$ — Directs input sources to assert $\overline{\text{TSTROBE}}$ as well as $\overline{\text{CSTROBE}}$ when sending data to the computer to provide a local copy on the screen of data entered into the computer.

$\overline{\text{LOCAL}}$ — Directs input sources to assert $\overline{\text{TSTROBE}}$ providing screen display in the absence of computer echo. The Interface(s) may also use this line. Originates in Keyboard switch.

$\overline{\text{SEND 8}}$ — Directs the Interface to accept full 8-bit binary data instead of providing its own data for the 8th bit. (The Keyboard does not provide an 8th bit of data.)

$\overline{\text{SWITCH 1}}$, $\overline{\text{SWITCH 2}}$ — Asserted by Keyboard switches SW1 and SW2. Their use is dependent upon program.

$\overline{\text{FUZZ}}$ — Causes the display to defocus the writing beam. Active during Alpha Mode.

$\overline{\text{INQUIRE}}$ — Set active when the ENQ Control Character is preceded by ESC. Sent by computer when requesting Terminal status.

$\overline{\text{CURSE}}$ — Set active when the SUB Control Character is preceded by ESC; Initiates Graphic Input Mode.

$\overline{\text{PAGE}}$ — Set active when the FF Control Character is preceded by ESC; also Page key. Causes the display to erase the screen. 1.6 microseconds wide minimum.

CR(H) — Causes X Register to set back to left side (Margin 0) of display.

$\overline{\text{MAKE COPY}}$ — Set active when the ETB Control Character is preceded by ESC. 866 μs width minimum. $\overline{\text{MAKE COPY}}$ can be activated by Make Copy switch on Keyboard.

$\overline{\text{INDICATOR 1}}$, $\overline{\text{INDICATOR 2}}$ — Turns on the light-emitting diode indicators in the Keyboard area.

NOTE

The above control characters are patchable except CR. Pulse width = 1.6 microseconds for all Control Characters.

$\overline{\text{BREAK}}$ — Signal from the Keyboard to the Interface for computer signaling.

NOTE

On some Interfaces, $\overline{\text{BREAK}}$ may be pulled up to +15 volts. Data signals may also be present on $\overline{\text{BREAK}}$.

$\overline{\text{SPEAK}}$ — Audio connection to the loudspeaker. Other terminal of speaker is at 5 volts. Bypassed by a 0.01 microfarad capacitor.

XMAT, YMAT — Analog signals representing the beam location within the character matrix. Originate on TC-1.

X, Y — Analog signals from TC-2 to display. −5 to +5 volts covers the screen. Positive signal corresponds to down and left deflection. 0 volts represents the physical center of the screen.

VIEW — Controls the flood guns in the CRT display unit. A high turns the guns on. As long as the Terminal is in Graphic Input or Hard Copy operation, and for about 90 seconds after the last information sent to the Terminal, TC-1 will allow a steady high on view. Otherwise, after 90 seconds, TC-1 places the display in "hold mode" by placing a 75 Hz signal with 12.5% duty factor on VIEW. An optional devices can place the display in non-store by pulling VIEW low.

614 kHz, 4.9 MHz — Clock signals.

WIRING INFORMATION

The following interconnecting references are provided to facilitate signal tracing:

Wire List—Explains signal paths through cables.

Connectors and Wiring Diagram—Depicts locations and identity of connectors.

Mother Board Diagrams (Connectors and Wiring Diagram)—Shows connector locations on Mother Board and lists interconnecting lines.

Display Interconnect Diagram—Shows chassis circuitry and Display Interconnect Board signal distribution.

From/To Addresses—Contained on schematics. List source or destination of subject signal. Does not list interconnecting points.

For most purposes, signal tracing consists of reading the address from the line on the schematic, and going to that location. Since all cards on the Mother Board (except A4) are interchangeable, addresses for these are simply listed as TO or FROM A3-BUS, followed by the specific pin number. These lines are applicable to all cards which can be inserted into the minibus connectors (TC-1, TC-2, Interface, Optional Extender).

In the event of cable trouble, it may be necessary to trace signals from point to point through all connectors. Start with the connector and pin number. If it is a harmonic connector, go to that connector in the Wire List. If it is a board-edge connector, go to that connector on the Mother Board diagram. Opposite the connector and pin number is listed the interconnecting point or points.

Examples of Signal Tracing

Example 1. Follow $\overline{\text{HIY}}$ from TC-1 to its destination. Since $\overline{\text{HIY}}$ is on an interchangeable board, its P202-J connector is common to pin J on all cards connected to the Mother Board, except A4 connected to J201. To determine if the signal goes elsewhere, look on the Mother Board diagram under minibus pin J. No other points are listed.

Example 2. Follow $\overline{\text{MAKE COPY}}$, which is generated on TC-1. Again, it is a connection on the minibus and goes to pin $\overline{\text{C}}$ on all minibus connectors. Look on TC-2 and the Interface card to determine if it is used there. Then check the Mother Board diagram. It shows that minibus pin $\overline{\text{C}}$ also connects to J201-B and J34-5. Going to J34 in the Wire List shows that pin 5 connects to P93 in A8. Refer to A8 on the Display Interconnect Diagram. The Display Interconnect Diagram discloses that it connects through J92-2 to the Make Copy switch, which also is a source for the signal. Since the Mother Board also indicated it connects to J201-B, go to the Connectors diagram (Fig. 6-1) and determine that P201 is on assembly A4. On the Hard Copy Adapter schematic (part of A4), find $\overline{\text{MAKE COPY}}$ and note that it leaves on J50-6. Refer to the Wire List and find that J50-6 goes to pin 11 of J525, the Hard Copy Unit connector plug.

Example 3. On the Keyboard schematic, locate KSTROBE on P80-6. Go to the Wire List and find that it connects to P21-2 on assembly A2, the TC-2 card. Referring to TC-2 confirms this.

WIRE LIST

From J1 and J2, CRT Connectors

Line Name	From		To		Location/ Assembly	Wire Color Code
	Plug and/or Jack	Pin	Plug and/or Jack	Pin		
W.G. FIL	1	1	Soldered to Board A5			9-1
W.G. FIL	1	2				9-2
W.G. Cathode	1	3				9-3
CONTROL	1	4				9-4
Focus	1	5				9-5
ANODE 1	1	6				9-6
ANODE 2	1	7				9-7
+20 V FIL	2	1	76		A6	2-3
−20 V	2	2	78		A6	7-1
CE 2	2	3	32	7	A3	9-5
S.T.B.	2	4	32	3	A3	9-2 Coax (See Note A)
F.G. ANODE	2	6	67	2	A5	9-4
F.G. CATHODE	2	7	32	5	A3	9-7
S.T.B. SHIELD	2	See Note B	32	1	A3	9-2 Coax Shield (See Note C)
Spare	2	NC	32	2	A3	9-1 Coax (See Note D)
Spare	2	NC	32	1	A3	9-1 Coax Shield (See Note D)

Note A: Was 2-N shielded in early instruments.

Note B: Soldered to 0-N wire which goes to ground lug on A-5.

Note C: Was 8-N shield in early instruments.

Note D: Not contained in early instruments.

WIRE LIST

From J20 and J21 Connectors on Assembly 2, TC-2 Circuit Card

Line Name	From		To		Location/ Assembly	Wire Color Code
	Plug and/or Jack	Pin	Plug and/or Jack	Pin		
GND	20	1	80	8	A7	0-N
X POT	20	2	99	6	A8	4-9
Y Pot	20	3	99	2	A8	9-2
b5	20	4	80	10	A7	9-18
b4	20	5	80	12	A7	9-26
b3	20	6	80	13	A7	9-28
b2	20	7	80	14	A7	9-27
b1	21	1	80	15	A7	9-25
KSTROBE	21	2	80	6	A7	9-24
b6	21	3	80	11	A7	9-17
+5 V (b8)	21	4	80	5	A7	9-16
b7	21	5	80	9	A7	9-23
SPARE	21	6	93	7	A8	9-35

WIRE LIST

From Connectors J30 and J31 on Assembly 3, Mother Board

Line Name	From		To		Location/ Assembly	Wire Color Code
	Plug and/or Jack	Pin	Plug and/or Jack	Pin		
						0-N
$\overline{\text{LOCAL}}$	30	1	93	8	A5	9-01
GND (Focus Shield)	30	2	62	1	A5	9-N } coax
DYNAMIC FOCUS	30	3	62	2	A5	9-N } coax
X DEF Coil (6-N)	30	4	63	2	A5	6-N
X DEF Coil (3-N)	30	5	63	3	A5	3-N
Hard Copy GND	30	6	100	2	A9	
$\overline{\text{HCU INT}}$	30	7	66	1	A5	9-12
$\overline{\text{TARSIG}}$	30	8	100	5	A9	9-13
$\overline{\text{Z}}$	30	9	65	2	A5	9-2 } coax
GND (Z Shield)	30	10	65	1	A5	9-2 } coax
+328 V	31	1	71	1	A6	9-5
+175 V	31	2	71	3	A6	9-0
DEF AMP GND	31	3	75		A6	0-N
GND	31	4	75	see note 1	A6	0-N
+20 V	31	5	76	see note 1	A6	2-35
−20 V	31	6	78	see note 1	A6	7-1
+5 V	31	7	72	see note 1	A6	2-0
+5 V	31	8	72	see note 1	A6	2-0
+15 V	31	9	70	see note 1	A6	2-1
−15 V	31	10	73	see note 1	A6	7-0

NOTE 1: These wires can be connected to any pin of their respective plug. For example, P31 pin 5 can be connected to any of P76 pins 1–3.

WIRE LIST

From Connectors J32, J33, and J34 on Assembly 3, Mother Board

Line Name	From		To		Location/ Assembly	Wire Color Code
	Plug and/or Jack	Pin	Plug and/or Jack	Pin		
GND (S.T.B. Shield)	32	1	2	Notes E & F		9-1 & 9-2 Coax Shield
S.T.B. Spare	32	2	2	See Note F		9-1 Coax
S.T.B.	32	3	2	4	CRT	9-2 Coax (See Note G)
F.G. ANODE	32	4	67	1	A5	9-4
F.G. CATHODE	32	5	2	7	CRT	9-7
$\overline{\text{FUZZ}}$	32	6	62	3	A5	9-36
CE-2	32	7	2	5	CRT	9-5
$\overline{\text{PAGE}}$	32	8	80	1	A7	9-34
$\overline{\text{SHIFT}}$	32	9	80	7	A7	9-6
$\overline{\text{SPEAK}}$	32	10	96	1	A8	9-3
Y DEF Coil (1-N)	33	1	63	1	A5	1-N
$\overline{\text{INDICATOR 1}}$	33	2	93	4	A8	9-04
$\overline{\text{INDICATOR 2}}$	33	3	93	3	A3	9-05
$\overline{\text{BREAK}}$	33	4	80	3	A7	9-14
$\overline{\text{CURSE}}$						
Y DEF Coil (4-N)	34	1	63	4	A5	4-N
$\overline{\text{HOME}}$ (Reset)	34	2	80	2	A7	9-15
$\overline{\text{SWITCH 1}}$	34	3	93	6	A8	9-02
$\overline{\text{SWITCH 2}}$	34	4	93	5	A8	9-03
$\overline{\text{MAKE COPY}}$	34	5	93	2	A8	9-06

Note E: Connects to ground on A5, via P2.
Note F: In early instruments, the shield from 32-1 and 0-N from 32-2 were connected together and tied to ground on A5.
Note G: Was a 9-2 in early instruments.

WIRE LIST

From Connectors J50 and J52 on Assembly 4, Deflection Amp & Storage Board

Line Name	From		To		Location/ Assembly	Wire Color Code
	Plug and/or Jack	Pin	Plug and/or Jack	Pin		
FAST RAMP	50	1	J525	3	Through cable to Hard Copy Unit.	2-N of 0-N COAX
FAST RAMP GND	50	2	J525	4		0-N of 8-N COAX
SLOW RAMP	50	3	J525	1		2-N of 8-2 COAX
SLOW RAMP GND	50	4	J525	2		0-N of 8-2 COAX
$\overline{\text{TARSIG}}$	50	5	J525	7		9-1 COAX
$\overline{\text{MAKE COPY}}$	50	6	J525	11		9-4
$\overline{\text{HCU}}$	50	7	J525	13		9-3
$\overline{\text{INTERROGATE}}$	50	8	J525	5		9-2 COAX
$\overline{\text{READ}}$	50	9	J525	9		0-9
GND	52	1,2,3,4	J525	CHASSIS gnd		0-N WIRE
	52	5 (not used)				
$\overline{\text{WAIT}}$	52	6*	J525	14		9-5

*Later models only: J53 on earlier models.

WIRE LIST

From J60, J61, J62, J63, J64, J65, J66 and J67 on Assembly 5, High Voltage Z Axis

Line Name	From: Plug and/or Jack	From: Pin	To: Plug and/or Jack	To: Pin	Location/ Assembly	Wire Color Code
GROUND (+20 V)	60	1	75	see note 1	A6	0-N
+20 V	60	2	76	see note 1	A6	2-N
GND	61	1	75	see note 1	A6	0-N
−15 V	61	2	73	see note 1	A6	7-0
+5 V	61	3	72	see note 1	A6	2-0
+15 V	61	4	70	see note 1	A6	2-1
+175 V	61	5	71	4	A6	9-0
+328 V	61	6	71	2	A6	9-5
GND	62	1	30	2	A3	9-N (coax)
DYNAMIC FOCUS	62	2	30	3	A3	9-N (coax)
$\overline{\text{FUZZ}}$	62	3	32	6	A3	9-36
Y DEF COIL	63	1	33	1	A3	1-N
X DEF COIL	63	2	30	4	A3	6-N
X DEF COIL	63	3	30	5	A3	3-N
Y DEF COIL	63	4	34	1	A4	4-N
Y DEF COIL	64	1				0-N
	64	2	Pin not present			
X DEF COIL	64	3*				2-N
X DEF COIL	64	4*				6-N
	64	5	(Pin not present)			
Y DEF COIL	64	6				4-N
GND	65	1	30	10	A3	9-0 (coax)
$\overline{\text{Z}}$	65	2	30	9	A3	9-0 (coax)
$\overline{\text{HCU INT}}$	66	1	30	7	A3	9-12
	67	1	32	4	A3	9-4
	67	2	2	6	CRT	9-4

*Early instruments have these two leads exchanged.

WIRE LIST

From J70, J71, J72, J73, J74, J75, J76, J77, J78, and J79 on Assembly A-6, Power Supply Board

Line Name	From		To			
	Plug and/or Jack	Pin	Plug and/or Jack	Pin	Location/ Assembly	Wire Color Code
+15 V	70	*1	31	9	A3	2-1
+15 V	70	*2	99	7	A8	2-1
+15 V	70	*3	61	4	A5	2-1
+20 V FIL	71	1	2	1	CRT	2-3
+328 V	71	2	31	1	A3	9-5
+328 V	71	3	61	6	A5	9-5
+175 V	71	4	31	2	A3	9-0
+175 V	71	5	61	5	A5	9-0
+5 V	72	1				
+5 V	72	2				
+5 V	72	*3	31	8	A3	2-0
+5 V	72	*4	61	3	A5	2-0
+5 V	72	*5	31	7	A3	2-0
+5 V	72	*6	80	4	A7	2-0
−15 V	73	*1	61	2	A5	7-0
−15 V	73	*2	31	10	A3	7-0
−15 V	73	*3	99	1	A8	7-0
	74	1			Heat Sink Q515 base	9-7

*Parallel connected on Power Supply board.

WIRE LIST

From J70, J71, J72, J73, J74, J75, J76, J77, J78, and J79 on Assembly A-6, Power Supply Board

Line Name	From		To		Location/ Assembly	Wire Color Code
	Plug and/or Jack	Pin	Plug and/or Jack	Pin		
	75	1				
GROUND	75	2	99	4	A8	0-N
GROUND	75	3	31	3	A3	0-N
GROUND	75	4	31	4	A3	0-N
GROUND	75	* 5		1	A3	0-N
GROUND	75	6				
GROUND	75	7	61	1	A5	0-N
GROUND	75	8				0-N } shield
GROUND	75	9				0-N } cut off
GROUND	75	10	60	1	A5	0-N
+20 V	76	1	60	2	A5	2-N
+20 V	76	2	31	5	A3	2-35
+20 V	76	3				
+15 V	77	1			Q510 Emitter	2-1
	77	2			Q510 Base	9-5
+20 V	77	3			Q510 Collector	2-3
−20 V	78	1	2	2	CRT	7-1
−20 V	78	* 2	31	6	A3	7-1
−20 V	78	3	empty			
−20 V	79	1			Q520 Emitter	7-1
−15 V	79	2			Q520 Collector	7-0
	79	3			Q520 Base	9-2

*Parallel connected on Power Supply board.

WIRE LIST

From J80, Assembly 7, Keyboard Circuit Card

Line Name	From		To		Location/ Assembly	Wire Color Code
	Plug and/or Jack	Pin	Plug and/or Jack	Pin		
$\overline{\text{PAGE}}$	80	1	32	8	A3	9-34
$\overline{\text{HOME}}$ (Reset Key)	80	2	34	2	A3	9-15
$\overline{\text{BREAK}}$	80	3	33	4	A3	9-14
+5 VDC	80	4	72		A6	2-0
+5 VDC (b8)	80	5	21	4	A2	9-16
+5 VDC (b8)	80	5	98	5	A8	2-0
KSTROBE	80	6	21	2	A2	9-24
$\overline{\text{SHIFT}}$	80	7	32	9	A3	9-6
GND	80	8	20	1	A2	0-N
b7	80	9	21	5	A2	9-23
b5	80	10	20	4	A2	9-18
b6	80	11	21	3	A2	9-17
b4	80	12	20	5	A2	9-26
b3	80	13	20	6	A2	9-28
b2	80	14	20	7	A2	9-27
b1	80	15	21	1	A2	9-25

*Connected on keyboard end.

WIRE LIST

From J92, J93, J94, J95, J96, J97, J98, and J99
Assembly 8, Display Interconnect

Line Name	From		To		Location/ Assembly	Wire Color Code
	Plug and/or Jack	Pin	Plug and/or Jack	Pin		
Spare	92 see note 2	1				
$\overline{\text{MAKE COPY}}$		2			S538 Rocker Switch on Keyboard	9-06
$\overline{\text{INDICATOR 2}}$		3			Ind 2 cathode (plug)	9-05
$\overline{\text{INDICATOR 1}}$		4			Ind 1—cathode (plug)	9-04
$\overline{\text{SWITCH 2}}$		5			S537 Rocker Switch on Keyboard	9-03
$\overline{\text{SWITCH 1}}$		6			S536 Rocker Switch on Keyboard	9-02
Spare		7				
$\overline{\text{LOCAL}}$		8			LOCAL/LINE Switch	9-01
Spare		1				
$\overline{\text{MAKE COPY}}$		2	34	5	A3	9-06
$\overline{\text{INDICATOR 2}}$		3	33	3	A4	9-06
$\overline{\text{INDICATOR 1}}$		4	33	2	A3	9-04
$\overline{\text{SWITCH 2}}$		5	34	4	A3	9-03
$\overline{\text{SWITCH 1}}$		6	34	3	A3	9-02
Spare		7	21	6	A2	9-35
$\overline{\text{LOCAL}}$	93 see note 2	8	30	1	A3	9-01
(CR542 SOURCE)	94	1			Indicator 2 anode (plug)	9-16
(CR540 SOURCE)	94	2			Indicator 1 anode (plug)	9-15
(CR544 SOURCE)	94	3			Power Indicator (plug)	9-14

***NOTE 2: P92 and P93 may be interchanged on A8 without effect.**

WIRE LIST

From J92, J93, J94, J95, J96, J97, J98, and J99
Assembly 8, Display Interconnect

Line Name	From		To		Location/ Assembly	Wire Color Code
	Plug and/or Jack	Pin	Plug and/or Jack	Pin		
−15 VDC	95	1	100	3	A9	7-0
GND	95	2	100			
+5 VDC	95	3	100	4	A9	2-0
+15 VDC	95	4	100	1	A9	2-1
$\overline{\text{SPEAK}}$	96	1	32	10	A3	9-3
Empty	96	2				
$\overline{\text{SPEAK}}$	97	1			Speaker	9-56
+5 V	97	2			Speaker	2-0
−15 V	98	1			Both Pots	7-0
Y Pot	98	2			Y Pot	9-2
	98	3				
GND	98	4			S1, 2, 3	0-N
+5 V	98	5	80	5	A7	2-0
X Pot	98	6			Y Pot	4-9
+15 V	98	7			Both Pots	2-1
−15 V	99	1	73	see note 1	A6	7-0
Y Pot	99	2	20	3	A2	9-2
	99	3				
GND	99	4	75	see note 1	A6	0-N
+5 V	99	5	80	5	A7	2-0
X Pot	99	6	20	2	A2	4-9
+15 V	99	7	70	see note 1	A6	2-1

see note 3

see note 4

NOTE 3: P96 and P97 can be interchanged on A8 without effect.
NOTE 4: P98 and P99 can be interchanged on A8 without effect.

WIRE LIST

From J100, J110, and J115, Assembly 9 (4010-1) TARSIG Hard Copy Amplifier

Line Name	From		To		Location/ Assembly	Wire Color Code
	Plug and/or Jack	Pin	Plug and/or Jack	Pin		
+15 V	100	1	J95	4	A8	2-1
Hard Copy GND	100	2	30	6	A3	
−15 V	100	3	J95	1	A8	7-0
+5 V	100	4	J95	3	A8	2-0
TARSIG	100	5	30	8	A3	9-13
Connects to P2 (CRT neck)	110					
Connects to J2 (cable)	115					
+20 V (Regulated Fil.)	110	1	2	1	TO CRT	
−20 V	110	2	2	2		
CE (1)	110	3	2	3		
STB	110	4	2	4		
CE (2)	110	5	2	5		
FG ANODE	110	6	2	6		
FG Cathode	110	7	2	7		
+20 V	115	1	2	1	To Deflection Amp and Storage Board, A4	
−20 V	115	2	2	2		
	115	3	2	3		
STB	115	4	2	4		
CE	115	5	2	5		
FG ANODE	115	6	2	6		
FG CATHODE	115	7	2	7		

WIRE LIST

From J525, Output Connector

Line Name	From		To		Location/ Assembly	Wire Color Code
	Plug and/or Jack	Pin	Plug and/or Jack	Pin		
SLOW RAMP	J525	1	50	3		2-N of 8-2 COAX
SLOW RAMP GND	J525	2	50	4		0-N of 8-2 COAX
FAST RAMP	J525	3	50	1		2-N of 8-N COAX
FAST RAMP GND	J525	4	50	2		0-N of 8-N COAX
$\overline{\text{INTERROGATE}}$	J525	5	50	8		9-2 COAX
$\overline{\text{INTERROGATE GND}}$		6				
$\overline{\text{TARSIG}}$	J525	7	50	5		9-1 COAX
$\overline{\text{TARSIG GND}}$		8				
$\overline{\text{READ}}$	J525	9	50	9		0-9
$\overline{\text{MAKE COPY}}$	J525	11	50	6		9-4
$\overline{\text{HCU}}$	J525	13	50	7		9-3
$\overline{\text{WAIT}}$	J525	14	52	6		9-5
GND	J525	15	52	1,2,3,4		0-N

BASIC CONCEPTS OF COMPUTER/TERMINAL COMMUNICATIONS (Refer to DATA FLOW BLOCK DIAGRAM)

General

The 4010 Computer Display Terminal is a device that permits a person to deal directly with a computer. (All references to the 4010 apply equally to the 4010-1. Where reference is to the 4010-1 only, it will be stated as such.) By using the Keyboard, which is similar to a typewriter keyboard, a person can question or instruct the computer and the computer's response is returned to that person by way of the display screen, either alphanumerically or graphically (charts, graphs, pictures, etc.).

The Terminal/Computer Communications block diagram is shown in the Data Flow block diagram. The different sections are the Computer, the Terminal (which includes the Keyboard, the Display Unit, and the Terminal Control circuitry) and the Communication Link.

Computer

The Computer can speak and act only through the use of binary numbers. The job of the Computer then, is to accept the data from the Terminal (commands from the Keyboard or other input devices), act on it by performing the indicated instruction and return its response to the Terminal.

Terminal

The Terminal acts as a translator between the operator and a computer. Its job is to take the data from the computer and translate it into a language or graphic form that makes the data understandable to the operator. This is the function of the 4010 Computer Terminal.

Display Unit. The Display Unit presents data visually for both alphanumeric and graphic operation by accepting X and Y (writing beam position) and Z (writing beam on or off) signals from the Terminal Control circuitry. These signals combine in the Display Unit to give a visual representation on the display screen of the data interchange between the operator and the Computer.

The 4010 Display Unit contains a storage-type CRT (cathode ray tube). The data being displayed has only to be written once. The characteristics of the storage tube allow the image of the data to be retained for a long period of time (up to one hour without damage to the display screen) without having to continually redraw it, as would be necessary if a television-type CRT were used.

Keyboard. The Keyboard provides the operator with a readily understandable means of inputting data to the Computer. It is an electromechanical device which, as a result of the operator's depressing any one of its keys, produces a binary data word that is distinctive for that key. This binary representation of the key depressed provides the Terminal Control Logic and the Computer circuits with a form of data they can understand.

Terminal Control Logic. This circuitry accepts data from either the Computer or the Keyboard. This circuitry also provides synchronization so that the data is handled in the proper sequence. When data is accepted by the Terminal Control Logic circuits, it routes this data to the Computer and/or the Terminal Display Unit, depending upon the data source and the function requested by the data. The Terminal Control Logic circuits interpret this data as either an alphabetic character or number, as coordinate points on an X-Y axis (for beam positioning), as a special function to be performed (backspace, ring bell, etc.) or as mode control information. Another function of the Terminal Control Logic is to allow the X and Y coordinates of any point on the display area of the screen to be sent from the Terminal to the Computer when commanded to do so.

Communication Link

Direct. When the Computer is located near the Terminal (as in the same building), a direct hook-up is the most practical. This type of communication link can best be thought of as simply plugging the Terminal into the Computer, just as you would plug a radio into a wall socket.

Modem (telephone hook-up). In most cases the computer will be located a considerable distance from the Terminal, making a direct connection impractical. In such cases, the transfer of information between the Computer and Terminal must be by other means. The most convenient and readily available means of transmission is the standard telephone and telephone lines. However, the Terminal and Computer cannot be hooked directly to the telephone because of the low frequency response of the telephone lines; therefore, the telephone hook-up consists of a modulator-demodulator (MODEM) which enables (modulates) the data on a voice frequency tone for transmission over the lines and decodes (demodulates) the data at the receiving end. Both the computer end and the Terminal end of the telephone line have MODEMS. Both ends operate the same. Thus, by the use of telephone lines and the MODEM, the distant computer can be reached as easily as dialing your next door neighbor.

DATA FLOW BLOCK DIAGRAM DESCRIPTION

General

The 4010 logic operation is controlled by three logic cards. These are TC-1, TC-2, and Computer Interface. Each card has 72 interconnecting pins. The same pins on each card are connected to one another by a plug-in connector board. This connector board is called a minibus. The minibus is designed to accommodate transmission between any devices connected to it.

Data is placed on seven data lines with open collector TTL buffers. The destination of data is determined by the use of strobe signals. Asserting a computer strobe ($\overline{\text{CSTROBE}}$) causes data to be transmitted to the computer. Asserting a terminal strobe ($\overline{\text{TSTROBE}}$) causes data to be transmitted to the Terminal. Data may be sent to both by asserting $\overline{\text{CSTROBE}}$ and $\overline{\text{TSTROBE}}$ simultaneously. Strobe signals are normally synchronized with the system clock (614 kHz).

Timing of data is controlled by $\overline{\text{TBUSY}}$ (terminal busy), $\overline{\text{CBUSY}}$ (computer busy). $\overline{\text{TBUSY}}$ and $\overline{\text{CBUSY}}$ control the rate of data transmission to devices responding to $\overline{\text{TSTROBE}}$ and $\overline{\text{CSTROBE}}$ respectively. The device receiving the data must enable its busy signal before the trailing edge of its respective input strobe if it is to be considered busy. If the device transmitting the data does not sense a busy signal before the trailing edge, it may presume that the data was accepted and present the next data immediately.

$\overline{\text{CPUNT}}$ (controlled by the interface), controls the interleaving of data transmission. Interleaving is the process of data being transmitted in either direction (to the computer, or from the computer) on the same data lines. Data from the computer is preceded by $\overline{\text{CPUNT}}$ to inhibit the Terminal and any other device (other than the interface card) from placing data on the minibus.

The 4010 operates in any of three basic modes.

Alphanumeric Mode (Alpha). An operating mode that transmits or displays alphanumeric characters and symbols for information purposes (address files, etc.).

Graphic Plot Mode (Graph). An operating mode that displays information in graphic form (graphs, charts, pictures, etc.).

Graphic Input Mode (Gin). An operating mode that provides the computer with a specific location on the display screen. Entails the generation of a "crosshair" cursor.

Alpha Mode

Keyboard Entered Data. Refer to the Data Flow Block Diagram. When the User enters data at the Keyboard, the key pressed is coded in its ASCII equivalent and sent to the Multiplexer on seven parallel lines, b1-b7. A Keyboard strobe signal termed KSTROBE accompanies the Keyboard bits to the Multiplexer. KSTROBE causes the computer strobe signal ($\overline{\text{CSTROBE}}$) to go active, and causes the Multiplexer to place the keyboard bits on the minibus as $\overline{\text{BIT 1}}$–$\overline{\text{BIT 7}}$. Then, $\overline{\text{CSTROBE}}$ strobes the bits through the Interface Card and to the computer. If the $\overline{\text{ECHO}}$ signal from the Interface Card is low, $\overline{\text{TSTROBE}}$ goes active along with $\overline{\text{CSTROBE}}$. This allows the 4010 circuitry to generate a "local" copy of the data sent to the computer. This occurs in the following manner.

$\overline{\text{TSTROBE}}$ enters the Column Decoder to allow $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ to generate an $\overline{\text{ALPHA STROBE}}$ signal. This signal latches the character code bits $\overline{\text{BIT 1}}$–$\overline{\text{BIT 5}}$ and $\overline{\text{BIT 7}}$, into the Character Generator. The Character Generator then decodes the bits and sends X and Y Matrix signals to the X and Y Digital to Analog circuits. $\overline{\text{TBUSY}}$ goes active at the same time, preventing reception of more data until the character is drawn. The X and Y DEFLECTION signals to the Display change in accordance with the X and Y MATRIX signals. The Z AXIS signal causes the display beam to either write or not write each specific X-Y Matrix coordinate. The composite of written points forms the desired character.

If the data bits contain the code for a Control Character, it is indicated by the $\overline{\text{BIT 6}}$–$\overline{\text{BIT 7}}$ combination, and detected by the Column Decoder. The Column Decoder then outputs a $\overline{\text{CTRL CHAR STB}}$ signal to the Control Character Decoder. This circuit decodes $\overline{\text{BIT 1}}$–$\overline{\text{BIT 5}}$ and outputs the function signal called for to the Format Effector. The Format Effector then initiates the function. For example, if the data bits contain the code for a SPACE, the Format Effector outputs the required number of pulses on the $\overline{\text{RIGHT}}$ line. At the same time, $\overline{\text{TBUSY}}$ goes active until the function is completed ($\overline{\text{TBUSY}}$ performs the same function as previously explained). These pulses increment the digital output of the X Register, causing the output of the X and Y Digital to Analog circuit to change accordingly. Thus, the display beam repositions one space.

Referring back to the Keyboard, you will notice a signal termed $\overline{\text{LOCAL}}$ that inputs to the Multiplexer. If the Local/Line switch is in Local, $\overline{\text{LOCAL}}$ goes active and $\overline{\text{CSTROBE}}$ is inhibited. No data can be sent to the computer under this condition. Only $\overline{\text{TSTROBE}}$ will go active to produce results as previously explained.

Computer Entered Data. Data from the computer enters the Interface Card. The Interface Card then generates $\overline{\text{TSTROBE}}$ and $\overline{\text{CPUNT}}$. $\overline{\text{CPUNT}}$ is a signal that precedes the computer data to the minibus. Its purpose is to prepare the Terminal for data reception. Depending upon the code of the data bits, they are either strobed into the Control Character Decoder or the Character Generator. The Terminal logic then processes the data as previously explained. Notice that $\overline{\text{TBUSY}}$ inputs to the Interface Card. $\overline{\text{TBUSY}}$ is generated by the Format Effector and/or the Character Generator to inhibit data reception from the computer until the Terminal completes the function.

Graphic Plot Mode

General. The Graphic Plot Mode permits lines (vectors) to be drawn on the CRT by addressing the beam to a point on the display screen. As the beam moves to that point, the Z Axis signal goes active to draw the vector.

Since the X and Y Registers each contain ten bits, twenty bits are required to address a certain position. These must be received in four bytes of five bits each, with each byte accompanied by two bits of steering data. The steering bits indicate X or Y, as well as whether the byte should be loaded as five most significant bits or five least significant bits. Data flow in the Graphic Plot Mode occurs in the following manner.

Refer to the Data Flow Block Diagram. When the Control Character bits for a GS that set the Graphic Plot Mode are received by the Interface Card, $\overline{\text{TSTROBE}}$ and $\overline{\text{CPUNT}}$ go active. $\overline{\text{BIT 1}}$–$\overline{\text{BIT 7}}$ are then placed on the minibus. The Column Decoder is activated by $\overline{\text{TSTROBE}}$ and detects from $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ that a Control Character has been received. It then causes the $\overline{\text{CTRL CHAR STB}}$ signal to activate the Control Character Decoder, which then decodes the remaining data bits ($\overline{\text{BITS 1–5}}$) and initiates the Special Function signals that set Terminal logic for Graphic Plot Mode. The next data bits received from the computer contain the first five bits of the coordinate address. $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ are decoded by the Column Decoder and the $\overline{\text{BYTE LOAD}}$ goes active, loading in $\overline{\text{BIT 1}}$–$\overline{\text{BIT 5}}$ into the Graphic Data Latches. The next two bytes are received and loaded into the Latches in the same manner. With the reception of the fourth byte, all twenty bits of data are loaded into the X and Y Registers (10 into the X Register, and 10 into the Y Register). This causes the digital output of the X and Y Registers to change suddenly to the value set by the twenty bits of input data, causing the output of the X and Y Digital-to-Analog circuits to change accordingly. At the same time the 20 bits of data are loaded into the X and Y Registers, the fourth $\overline{\text{BYTE LOAD}}$ pulse from the Column Decoder enables the Format Effector to output a $\overline{\text{Z}}$ Vector Enable signal. This turns on the display beam while the X and Y DEFLECTION signals change, causing a vector to be written. When the Vector Enable signal goes active, $\overline{\text{TBUSY}}$ also goes active to prevent the reception of more data from the computer until the vector is drawn.

Graphic Input Mode (GIN)

General. The Graphic Input Mode is used to send graphic data to the computer. This entails the generation of a full-screen cross-hair cursor that can be positioned to any point on the viewable display area. The positioning of the cross-hair cursor is performed by the use of two position controls (potentiometers) which are located to the right of the Keyboard.

Refer to the Data Flow Block Diagram. The initiation of the GIN Mode occurs in much the same manner as the Graphic Plot Mode. The Control Characters (ESC and SUB) that initiate the GIN Mode are received from the computer and cause the Control Character Decoder to output a $\overline{\text{CURSE}}$ signal that is sent to the Cross-hair Generator. The cross-hair cursor is then drawn on the screen of the CRT in the following manner.

When initialized by the $\overline{\text{CURSE}}$ signal from the Control Character Decoder, the Crosshair Generator circuit sends $\overline{\text{DOWN}}$ pulses to the Y Register. These pulses cause the Y Register to increment, moving the display beam downward. As the Y Register increments with each pulse from the Crosshair Generator, the Y Digital output changes accordingly. The Y Digital-to-Analog Circuit converts the Y Digital input to its comparative analog value, outputting it as the Y DEFLECTION voltage to the Display Unit. With each pulse, the Crosshair Generator sets the Z Axis line active to draw the point. Notice that the X and Y DEFLECTION voltages are being sampled by the Crosshair Generator. When the deflection voltage just passes the voltage being input from the Y Position Pot, the Crosshair Generator switches the count to the X axis. The Y Register maintains its value while the X Register is being incremented by $\overline{\text{RIGHT}}$ signals from the Crosshair Generator. Like the Y Register, it increments until the X Deflection voltage just passes the voltage input from the X Position Pot. When this occurs, the circuit once again switches to the Y Register. The above-stated sequence repeats itself until the Terminal receives a command to send the intersection point to the computer.

The sending of the data to the computer can be done under User control, or computer control.

When the User wishes to send the intersection point, he strikes a Keyboard key. The Keyboard character bits go to the computer as explained in the description of Alpha Mode operation. The Terminal will not be affected, because the Multiplexer does not generate a $\overline{\text{TSTROBE}}$ signal.

$\overline{\text{CBUSY}}$ goes active during the time that it takes the computer to receive the Keyboard character data bits. When the computer completes the receiving process, $\overline{\text{CBUSY}}$ goes inactive. This causes the Multiplexer to send an active $\overline{\text{GO DIGITIZE}}$ signal to the Crosshair Generator. The next time the Crosshair Generator reaches the intersection point it stops the counting sequence. The X and Y Registers are held at the digital equivalent of the X and Y Position Pot analog voltages. When the counting sequence stops, the Crosshair Generator sends a $\overline{\text{PT FOUND}}$ signal back to the Multiplexer. This causes the Multiplexer to send the 20 bits of X and Y Digital information to the minibus in four bytes. With each 5-bit byte, the Multiplexer sets $\overline{\text{BIT 6}}$-$\overline{\text{BIT 7}}$ low and generates the $\overline{\text{CSTROBE}}$ signal. This causes the data to be sent to the computer.

The computer can also request the coordinates of the Cross-hair Cursor by sending the Control Character ESC followed by the Control Character ENQ (Inquire). When ENQ is decoded by the Control Character Decoder, the $\overline{\text{INQUIRE}}$ signal to the Multiplexer goes high. The operation of the Graphic Input circuitry is then the same as if $\overline{\text{CBUSY}}$ went inactive after a Keyboard character had been sent.

ALPHA MODE BLOCK DIAGRAM DESCRIPTION

General. When operating in the Alpha Mode, the 4010 presents data in the form of alphanumeric characters and special symbols. It can display a total of 63 different characters. Although lower-case alphabetic characters can be received, they are written as upper-case. Some of the characteristics of the Alpha Mode are as follows:

1. The characters are generated by a 5 X 8 dot matrix contained within a Read Only Memory (ROM) device (the Character Generator uses only 7 of the 8 available "row" outputs of the ROM). The ROM has 64 character selection capability, with one character (DEL) being suppressed.

2. Alphanumeric data can be displayed on 35 lines, with each line containing up to 74 characters.

3. The Alpha Cursor is a pulsating 5 X 7 dot matrix that indicates where the next character will be displayed.

4. There are two margins, termed Margin 0 and Margin 1. Margin 0 is the left side of the display screen and Margin 1 is the vertical center of the display screen.

5. The Terminal performs an automatic Carriage Return/Line Feed when spacing past the end of a line.

The main purpose of the Alpha Mode Description is to show how the Terminal processes alphanumeric data for display purposes.

Power Initialization. Refer to the Alpha Mode Block Diagram. When power is first applied, the Home circuit (located in the upper-left corner of the diagram) applies a low on the $\overline{\text{HOME}}$ line, placing the Terminal in Alpha Mode. Further switching to Alpha Mode occurs in the following manner.

When $\overline{\text{HOME}}$ goes low, it causes the Graf Flipflop to set $\overline{\text{NOLT}}$ active. With $\overline{\text{NOLT}}$ active, the X and Y Filters are disabled, permitting the X and Y Analog voltages to pass through to the Deflection Amplifier circuitry unaffected. $\overline{\text{NOLT}}$ also enters the Column Decoder to allow three different combinations of $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ to generate the $\overline{\text{ALPHA STB}}$ signal.

Referring back to the $\overline{\text{HOME}}$ signal, notice that it also causes the output of U69C to go high. This clears the X and Y Registers, causing the display beam to position to Home (upper-left corner of the Display screen). A few milliseconds after initialization, when the power has stabilized, the $\overline{\text{HOME}}$ signal goes inactive.

The display screen attains a "fully written" condition at turn-on. The screen must be erased before entering any data. This is accomplished by pressing the Page key. This causes the screen to be erased and set to the normal viewing level. (For effect of $\overline{\text{PAGE}}$ on display circuits, refer to the Display Unit Block diagrams and descriptions.)

Processing Control Characters. When the data bits of a Control Character are placed on the minibus, the $\overline{\text{TSTROBE}}$ signal is generated. $\overline{\text{TSTROBE}}$ activates the $\overline{\text{TERM STB}}$ signal from the Terminal Strobe Gating circuit. The $\overline{\text{TERM STB}}$ signal enables the Column Decoder to process $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ (both are high when the data bits contain the code for a Control Character) and output an active Control Character Strobe ($\overline{\text{CTRL CHAR STB}}$) signal. This signal is used to enable the Control Character Decoder. Data bits $\overline{\text{BIT 1}}$–$\overline{\text{BIT 4}}$ and $\overline{\text{BIT 5}}$ and its complement, input to the Control Character Decoder. The Control Character Decoder then decodes the input data and activates the respective output line. For example, the Line Feed (LF) Control Character bits activate the $\overline{\text{LF}}$ signal.

The Escape circuit is shown as part of the Control Character Decoder circuit. This circuit makes it more difficult to accidentally generate one of four special output signals – $\overline{\text{PAGE}}$, $\overline{\text{CURSE}}$, $\overline{\text{MAKE COPY}}$, and $\overline{\text{INQUIRE}}$. These signals are the result of a two-Control Character sequence. First, the Escape (ESC) Control Character is received to prepare the Escape Circuit for the next Control Character. This is followed by the command that selects the specific function. For example, to activate the $\overline{\text{MAKE COPY}}$ signal (which activates the Hard Copy Unit) the ESC Control Character is first received; it is followed by the ETB (End of Tape Block) Control Character. The decoding of ETB by the Control Character Decoder then causes the Escape Circuit to activate the $\overline{\text{MAKE COPY}}$ signal. The remaining three output signals from the Escape Circuit are similarly activated: ESC and FF (Form Feed) activate PAGE; ESC and SUB (Substitute) activate $\overline{\text{CURSE}}$ and ESC and ENQ (Inquire) activate $\overline{\text{INQUIRE}}$. The Escape circuit is cleared when the CLEAR signal from the Terminal Strobe Gating circuit goes active. This occurs when the $\overline{\text{TSTROBE}}$ signal ends, unless the ESC character is being input. This means that the character following ESC disarms the circuit, regardless of whether or not it contains one of the commands of execution.

The signals from the Control Character Decoder are input to the Format Effector. The input signals $\overline{\text{HT}}$, $\overline{\text{BS}}$, $\overline{\text{LF}}$, and $\overline{\text{VT}}$ direct it to output a predetermined number of pulses on either the $\overline{\text{RIGHT}}$, $\overline{\text{LEFT}}$, $\overline{\text{DOWN}}$, or $\overline{\text{UP}}$ signal lines. To backspace the Alpha Cursor, the BS Control

Character must be sent. BS causes the Control Character Decoder to activate the $\overline{BS}$ signal. $\overline{BS}$ then causes the Format Effector to output 14 pulses on the $\overline{LEFT}$ line. At the same time, $\overline{TBUSY}$ goes active, holding the Terminal in a "BUSY" condition until the function is completed. These pulses decrement the output of the X Register 14 counts, causing the output of the X Digital to Analog circuit to change its analog output value accordingly. This new value of X ANALOG voltage passes unaffected through the X Filter circuit (the Filter circuits are inhibited by $\overline{NOLI}$) and causes the X Deflection Amplifiers to deflect the display beam one space to the left. Similar action occurs when the Terminal receives a Horizontal Tab (HT) Control Character. The only difference is that when HT is decoded, the $\overline{HT}$ signal goes active, causing the Format Effector to pulse the $\overline{RIGHT}$ line 14 times. The X Deflection Amplifier then deflects the display beam one space to the right.

To move the display beam up or down, the Vertical Tab (VT) or the Line Feed (LF) Control Characters must be sent. $\overline{VT}$ causes the Format Effector to pulse the $\overline{UP}$ line 22 times. $\overline{LF}$ causes the Format Effector to pulse the $\overline{DOWN}$ line 22 times. The resultant action from the Y Register through the Y Digital to Analog and Y Filter circuits is similar to that of the X Register. The end result is to move the display beam either up or down one line of type.

When any of the input lines to the Format Effector go active, $\overline{TBUSY}$ is also activated. $\overline{TBUSY}$ is used by the Computer Interface Card to slow down the transmission rate from the computer to allow the Terminal time to process the data. The standard 4010/4010-1 is capable of receiving and processing alphanumeric data up to 9600 baud. $\overline{TBUSY}$ must be used for higher baud rates.

Control Characters such as BEL and CR cause the Format Effector to activate $\overline{TBUSY}$ for a predetermined period of time. $\overline{BEL}$ causes the Format Effector to output a 1200 Hz bell signal on the $\overline{SPEAK}$ line. When the predetermined span of time has elapsed, the Format Effector ends the $\overline{SPEAK}$ signal and at the same time ends $\overline{TBUSY}$. The $\overline{CR}$ signal causes the Format Effector to output the CR signal and at the same time sets $\overline{TBUSY}$ active. CR inputs on the CLEAR input of the X Register, setting its outputs and the display beam to the predetermined margin position.

If $\overline{GS}$ has set the Graphic Plot Mode, the Alpha Mode can be re-established by sending any of the following Control Characters: US, CR, or ESC and FF ($\overline{PAGE}$). Pressing the Page or Reset keys will also re-establish the Alpha Mode. The above signals are input to the Graf FF to set $\overline{NOLI}$ active and $\overline{GRAF}$ inactive. The Format Effector activates $\overline{TBUSY}$ to give the Terminal logic time to reset to the Alpha Mode.

Processing Alphanumeric Characters. The Character Generator circuitry is capable of generating 63 distinct alphanumeric characters and special symbols. When no characters are being generated, the Character Generator outputs signals that draw a pulsating 5 X 7 dot matrix. This is the alpha cursor which indicates the beam writing position. The operation of the Character Generator is as follows.

When $\overline{TSTROBE}$ goes active, upon receipt of a character, the Terminal Strobe gating circuit activates the $\overline{TERM\ STB}$ signal. $\overline{TERM\ STB}$ causes the Alpha Cursor Suppress circuit to set the SUPPRESS signal active. The SUPPRESS signal presets the Y Matrix (Y MAT) and X Matrix (X MAT) signals to put the display beam in the proper position to begin drawing the character.

The $\overline{TERM\ STB}$ signal also activates the Column Decoder which decodes $\overline{BIT\ 6}$ and $\overline{BIT\ 7}$ and outputs the Alpha Strobe ($\overline{ALPHA\ STB}$) signal. This allows the Character Generator to receive the $\overline{BIT\ 1}$–$\overline{BIT\ 5}$ and $\overline{BIT\ 7}$ data bits, and at the same time sets the Character in Progress ($\overline{CHAR\ IN\ PROG}$) signal active. The $\overline{CHAR\ IN\ PROG}$ signal causes the Format Effector to set $\overline{TBUSY}$ active, thus preventing the reception of more data until the drawing of the character is completed.

Each of the 63 distinct characters that the Character Generator can produce has its own 5 X 7 dot matrix within a Read Only Memory (ROM) device in the Character Generator. The data bits ($\overline{BIT\ 1}$–$\overline{BIT\ 5}$, $\overline{BIT\ 7}$) are used to address the matrix of the specified character or symbol within the ROM. Timing signals from the Format Effector then cause the Character Generator to scan through the matrix one dot at a time. As the Character Generator scans the matrix, it outputs the X MAT and Y MAT analog voltages. These voltages are input to their respective Digital to Analog circuits to cause the Deflection Amplifier circuitry to position the display beam through the 5 X 7 dot matrix.

As the ROM matrix is scanned, it indicates if a dot is to be written or not. The dot to be written causes the $\overline{WRITE\ DOT}$ signal to the Format Effector to go active. The Format Effector then outputs an active $\overline{Z}$ signal that causes the display beam to write a dot. The composite of the unblanked matrix dots forms the specified character on the display screen.

When the Character Generator has completed scanning the matrix, the Character Complete ($\overline{CHAR\ COMP}$) signal goes active. This causes the Format Effector to output 14 pulses on the $\overline{RIGHT}$ line, thus, spacing the alpha cursor to the next character position. The $\overline{CHAR\ IN\ PROG}$ signal ends, ending $\overline{TBUSY}$. The Terminal can now receive the next byte of data.

View Signal Operation. The purpose of the VIEW signal is to prolong the life of the CRT. If no new data is being entered, this signal is modulated by a 75 Hz signal which provides a duty time of 12 1/2% for the VIEW signal. The result to the display screen is a dimming of the displayed data and the suppressing of the Alpha Cursor. The View Multi and Gating circuit operates in the following manner.

The View Multi is basically a one-shot multivibrator that, when triggered, allows the VIEW signal to remain high for approximately 90 seconds. The View Multi is triggered whenever any one of its various input control signals pulse high. If no activity occurs within 90 seconds, the VIEW signal from the View Multi ends. This action places the 75 Hz signal on the VIEW line. At the same time, the $\overline{\text{VIEW}}$ signal to the Alpha Cursor Suppress circuit goes active. $\overline{\text{VIEW}}$ holds the SUPPRESS signal active, suppressing the $\overline{\text{WRITE DOT}}$, X MAT and Y MAT signals that were drawing the alpha cursor. The entering of new data restores the data and the alpha cursor to view.

Alpha Cursor Suppress. Three signals that suppress the alpha cursor and hold VIEW high are:

$\overline{\text{DR BUSY}}$—Asserted by the Hard Copy Unit during character processing.

$\overline{\text{GRAF}}$—Asserted by the Graf FF during graphic operation.

$\overline{\text{GIN}}$—Asserted by the Multiplexer during Graphic Input Mode.

Character Generator Inhibit. This circuit is used to inhibit the Character Generator when $\overline{\text{GIN}}$ goes active. ($\overline{\text{GIN}}$ goes active when the mode of operation is set to Graphic Input Mode.) This prevents the Character Generator from responding to the $\overline{\text{ALPHA STB}}$ signal caused by sending the "Header Character" to the computer. The Header Character initiates the sequence of data bytes that contain the graphic data to be sent to the computer. For a more detailed explanation of the Graphic Input Mode, refer to the Graphic Operation Block Diagram Description.

The $\overline{\text{LOCAL}}$ signal from the Keyboard goes active when the Local/Line switch is in the Local position. This sets the $\overline{\text{INH}}$ signal inactive, allowing the Character Generator to respond to alphanumeric data entered from the Keyboard.

The $\overline{\text{TBUSY}}$ signal is also used to enable character generation. When the Graphic Plot Mode is activated the $\overline{\text{GS}}$ signal will pull the $\overline{\text{GIN}}$ line low, causing the $\overline{\text{INH}}$ signal to go active. If it is desired to display alphanumeric data in conjunction with Graphic Plot Operation, the Character Generator must be enabled. This is done by sending the CR or US Control Character to the Terminal, switching it to Alpha Mode. (Sending US allows the first alphanumeric character or symbol to be displayed at the ending point of the last vector.) $\overline{\text{TBUSY}}$ then goes active, causing the $\overline{\text{INH}}$ signal to go inactive, enabling the Character Generator to respond to $\overline{\text{ALPHA STB}}$ signals.

X Register. The X Register outputs 10 bits of BCD (binary coded decimal) data which provide a count from 0 to 1023. The Register is capable of counting up or down to any number within this range. Each bit of data is input to the X Digital to Analog on its own line (all ten lines are drawn as one on the Block Diagram). In Alpha Mode operation, the signals that increment and decrement the X Register are $\overline{\text{RIGHT}}$ and $\overline{\text{LEFT}}$ respectively. Each pulse increments or decrements the count by one. The X Register is cleared when power is first applied ($\overline{\text{HOME}}$ goes active) or a $\overline{\text{PAGE}}$ signal is received. This causes the CLEAR signal from U69C to set all 10 output bits low, causing the display beam to position to the left hand margin. When the count increments to 1023, an End of Line ($\overline{\text{EOL}}$) signal is sent to the Format Effector. This causes the Format Effector to output a CR signal, clearing the Register, once again causing the display beam to position to the left hand margin.

Y Register and Top-of-Page Detect Operation. The operation of the Y Register is similar to the X Register. The main difference is that when the Y Register is cleared, all its outputs go high; pulsing the $\overline{\text{DOWN}}$ line decrements the count; pulsing the $\overline{\text{UP}}$ line increments the count. Because the display screen is not as high as it is wide, not all the 1023 points are viewable, as they are for the X Register. Therefore, when the Y Register is cleared the alpha cursor is positioned off-screen beyond the top of the page. The purpose of the Top-of-Page Detect circuit is to decrement the count from the Y Register by pulsing the $\overline{\text{DOWN}}$ line until the top-of-page position is reached. The top-of-page position represents a Y Register count of 767, and is also known as the Home position for the Y Register. It operates in the following manner.

When the Y Register outputs a count greater than 767 (1023 when it is cleared), the two Most Significant Bits of the Y Register (2 MSBY) are high. This activates the Top-of-Page Detect circuit which begins pulsing the $\overline{\text{DOWN}}$ line. When the count of 767 is reached, the 2nd MSB of the Y Register goes low, inhibiting the $\overline{\text{DOWN}}$ pulses. Thus, the top-of-page has been detected and the Alpha Cursor is positioned in view at the top of the display screen.

Margin Shifter Operation. Left and Right margins are established as a result of the lower and upper limits of the X Register. There is another margin that can be established

at mid-page (X = 512) to provide an increased number of lines on which to enter data.

The Left Margin is referred to as Margin 0, the center margin as Margin 1. Margin 0 is always established as a result of $\overline{\text{PAGE}}$ or $\overline{\text{HOME}}$ signals. The establishing of Margin 1 occurs in the following manner.

When the last line of type for Margin 0 has been reached and all desired data entered on that line, a CR and an LF code bit must be received by the Terminal to position the Alpha Cursor to Margin 1. (The order in which they are sent is immaterial.)The LF causes the Y Register to space past the bottom line of type which sets the MARG signal to the X Register active (the MARG signal is actually an eleventh bit from the Y Register that carries a BCD weight of 1024). When it goes active, it causes the MSB of the X Register (512) to remain high. This causes Margin 1 to be set.

At the same time that LF causes MARG to go high, it causes the Top-of-Page circuit to activate. The Alpha Cursor then positions to the top of the page. But, this time the MSB from the X Register is held high, and the alpha cursor is at the top-of-page, center of screen. CR signals will not clear the Margin 1 position. This can be cleared by again spacing the Y Register past the bottom line of the page (unless break on page full has been strapped). When this occurs, the MARG signal goes inactive. Margin 1 can also be cleared by activating the $\overline{\text{HOME}}$ or $\overline{\text{PAGE}}$ signals.

Digital to Analog Conversion. The X and Y Digital to Analog (D/A) converter circuits operate similar to one another. Their purpose is to convert the digital output of their respective Registers into the equivalent analog voltage. These circuits also sum the X and Y analog MAT signals (from the Character Generator) with the X and Y analog signals, respectively. The outputs of these circuits pass directly through their respective Filter circuits (unaffected in Alpha Mode) and are input to the X and Y Deflection Amplifier circuitry to position the display beam.

GRAPHIC MODES BLOCK DIAGRAM

General

The 4010 processes graphic data in two formats. It can accept graphic data from the computer to draw vectors. This is termed Graphic Plot Mode. It can send graphic data to the computer. This is known as Graphic Input Mode.

Graphic data from the computer causes the 4010 to write vectors on the Display as specified by X and Y coordinate data. The 4010 requires 20 bits of data to represent the axis address (10 bits for X and 10 bits for Y). This data is supplied to the Terminal by the computer in 4 seven-bit bytes. The two most significant bits are steering data; the five least significant bits contain the coordinate information.

Graphic Plot Mode Description

Refer to the Graphic Operation Block Diagram. Graphic Plot Mode operation is as follows.

Graphic Mode Initialization. The 4010 logic is designed so that when the Terminal is first turned on, the Home circuit resets all logic to the Alpha Mode. Notice the Home circuit of the Block Diagram. When power is first turned on (initialized), it outputs a $\overline{\text{HOME}}$ signal. This causes the Graf F/F to output signals that set the Alpha Mode. $\overline{\text{GRAF}}$ goes high (inactive); $\overline{\text{NOLI}}$ goes low to inhibit the linear interpolation circuitry in TC-2. $\overline{\text{NOLI}}$ also inputs to the Column Decoder. Initialization of the Graphic Plot Mode begins with the Control Character GS. GS is usually initialized under program control, but can be sent from the Keyboard by pressing the CRTL and SHIFT and M keys simultaneously. For the purposes of this discussion, assume that the GS has been entered from the computer and is placed on the minibus.

When the GS data is placed on the minibus, $\overline{\text{TSTROBE}}$ goes active to enable the Terminal Strobe gating circuitry to input a low $\overline{\text{TERM STB}}$ signal to the Column Decoder. When $\overline{\text{TERM STB}}$ goes active, the $\overline{\text{CTRL CHAR STB}}$ signal is sent to the Control Character Decoder to allow it to process the GS data bits at its inputs. The Control Character Decoder outputs a low $\overline{\text{GS}}$ signal to the GRAF F/F. This action switches the output states of the F/F; $\overline{\text{GRAF}}$ goes low, and $\overline{\text{NOLI}}$ goes high. $\overline{\text{NOLI}}$ going high enables the X and Y Filter circuits.

Even though the $\overline{\text{NOLI}}$ input to the Column Decoder is high, the proper combinations of $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ will still generate the $\overline{\text{CTRL CHAR STB}}$. Thus, no matter whether operating in alpha or graphics, a $\overline{\text{CTRL CHAR STB}}$ can be generated to enable the Control Character Decoder.

Alpha Circuits Inhibited. In Graphic Plot Mode, the following Alpha Mode circuits are inhibited.

1. Character Generator
2. Auto CR/LF
3. View/Hold
4. Cursor Refresher
5. Top-of-Page Detect
6. Margin Shifter
7. Right Margin

Explanations on how the above circuits are inhibited will be given in that order.

With $\overline{\text{NOLI}}$ set high, the Column Decoder is prevented from outputting an active $\overline{\text{ALPHA STROBE}}$ signal to the Character Generator. With the $\overline{\text{ALPHA STROBE}}$ inhibited, $\overline{\text{BIT 1}}$–$\overline{\text{BIT 5, 7}}$ cannot be input to the Character Generator. $\overline{\text{GRAF}}$ also enters the Alpha Cursor Supress circuit to cause a high-going SUPPRESS signal that resets the Character Generator to the Column 0, Row 0 position of the Character Matrix. The $\overline{\text{77 kHz}}$ pulses that clock the Character Generator through the matrix are also inhibited. Thus, the Character Generator is prevented from applying any voltages to the X and Y Digital to Analog circuits that might cause displacement of the beam while drawing a vector.

The same SUPPRESS signal that disabled the Character Generator also disables the Auto CR/LF and View/Hold Circuits. As long as the SUPPRESS signal is high, $\overline{\text{LF}}$ signals from the Control Character Decoder will not activate an automatic carriage return and line feed function. The high SUPPRESS signal inhibits the View Hold circuit. This allows the displayed vectors to remain visible continually. (This is why the Terminal should be returned to Alpha mode immediately after any plotting is finished to allow the View Multi to time the display into Hold.) The SUPPRESS signal is also input to the Cursor Refresher circuit to inhibit the generation of the Alpha Cursor.

When $\overline{\text{GRAF}}$ goes low, the output of U67 inhibits the Top-of-Page Detect and Margin Shifter circuits.

Data Loading. $\overline{\text{BIT 1}}$–$\overline{\text{BIT 5}}$ are placed immediately at the input to the Y Data Latch with the arrival of the first coordinate data byte from the computer. $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ are decoded by the Column Decoder and Graphic Byte Decoder circuits. When the decoding occurs, $\overline{\text{HIY}}$ from the

Graphic Byte Decoder goes low and strobes the five most significant bits of the Y coordinate address into the appropriate portion of the Y latch. As each following byte arrives on the minibus, $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ are decoded to enable the Graphic Byte Decoder to Strobe the LOY and HIX bytes into their appropriate latches. With the arrival of the LOX byte, $\overline{\text{LOXE}}$ goes low. Notice that there is no latch for the LOX bits. The LOX bits are strobed directly into the X Register. With the arrival of the LOX Byte, the $\overline{\text{LOXE}}$ signal simultaneously loads all twenty bits of coordinate data into the X and Y Registers. This causes the output of the X and Y D/A's to immediately change to the new coordinate position. Now that the outputs of the X and Y D/As are at the new position, the X and Y Filters begin linearly changing the X and Y signals to the new values. The display beam must now be turned on to draw the vector.

Vector Enabling. $\overline{\text{LOXE}}$ also enters the Format Effector, Pulse Shaper and Vector Enable Blocks. In the Format Effector, $\overline{\text{LOXE}}$ is used as a preset input to time the 2.6 ms PAUSE signal that is used to activate the $\overline{\text{Z}}$ signal needed to draw the vector. The $\overline{\text{LOXE}}$ input to the Pulse Shaper generates the $\overline{\text{LOAD}}$ pulse that loads $\overline{\text{LOXE}}$ into the Format Effector. The first vector to be drawn is always dark; therefore, the VECTOR ENABLE output from the Vector Enable circuit is low, inhibiting the Z Axis circuit. With the arrival of the Low Order X bits of the next vector string, the VECTOR ENABLE signal goes high. This enables the Z Axis circuit to output an active $\overline{\text{Z}}$ signal to draw the vector. When the Format Effector has ended the 2.6 ms PAUSE signal, the $\overline{\text{Z}}$ signal is inhibited. Thus, the $\overline{\text{Z}}$ signal combined with the movement of the X & Y inputs from the Filter circuits causes the vector to be drawn.

A Z Control circuit is contained on TC-2 circuit cards No. 670-1729-05 and above. This chops the Z signal during short vector intensity more consistent with long vector intensity. The $\overline{\text{LOXE}}$, $\overline{\text{NOLI}}$, X D/A, Y D/A, and three clock signals (not shown) are fed into the circuit to hold $\overline{\text{CGZSUP}}$ high for vectors more than approximately one-half inch long, and to place a 12 1/2% duty cycle high on the $\overline{\text{CGZSUP}}$ line while vectors less than approximately one-half inch are being drawn.

Return to Alpha. When vector plotting is completed, it is best to return the 4010 to Alpha Mode. This allows the Terminal to time into Hold Mode to prevent possible damage to the Display Screen.

Alpha Mode is re-established by resetting the GRAF F/F. The following Control characters will set Alpha Mode: CR, US or ESC plus FF (PAGE).

In addition, the following Keyboard keys will reset the Terminal to Alpha Mode: Page or Reset.

Graphic Input Mode Description

Graphic Input Initialization. Graphic Input Mode is set by the Control Characters ESC plus SUB. When they are received and decoded by the Control Character Decoder, the Escape circuitry outputs the $\overline{\text{CURSE}}$ signal (see TC-1 discussion on Escape circuitry for description on operation of Escape). $\overline{\text{CURSE}}$ inputs to the GRAF F/F to set $\overline{\text{NOLI}}$ low and $\overline{\text{GRAF}}$ high. $\overline{\text{NOLI}}$ going low inhibits the X & Y Filter circuits, thus allowing the outputs of the X & Y Filter circuits to pass directly through the Filter circuits unaffected. $\overline{\text{CURSE}}$ is processed in the Multiplexer circuitry, causing output $\overline{\text{GIN}}$ to go active. When $\overline{\text{GIN}}$ goes active it causes the SUPPRESS signal from the Character Generator Suppress circuit to go high. The Automatic CR/LF, View/Hold, and Cursor Refresher circuits are inhibited as previously explained in Graphic Plot operation. $\overline{\text{GIN}}$ also inhibits the Graphic Byte Decoder during Graphic Input Mode. (The Column Decoder can still output the $\overline{\text{CRTL CHAR STB}}$ to the Control Character Decoder. Thus, Control Characters can still be processed.) The Top-of-Page Detect and the Margin Shifter circuits are also inhibited when $\overline{\text{GIN}}$ causes the output of U67 to go low. The 4010 logic circuitry is now set for Graphic Input operation.

Cross-Hair Generator. When $\overline{\text{CURSE}}$ goes low, the Cross-hair Generator is activated. When first activated, the Cross-hair Generator begins sending $\overline{\text{DOWN}}$ pulses to the Y Register. Each time it pulses, it sends a short $\overline{\text{Z}}$ pulse to turn on the display beam. As the Y Register output decrements, it causes the output of the Y D/A to change accordingly. Thus, the display beam begins moving in the down direction. The output of the Y D/A is being sampled by the Cross-hair Generator. When this voltage changes to the point where it just passes the voltage from the Y position Potentiometer, the counting pulses switch to the $\overline{\text{RIGHT}}$ line. This is known as "Y coincidence". The Y Register maintains its value while the X Register is incremented. The output of the X Register increments once with each low $\overline{\text{RIGHT}}$ pulse, causing the output of the X D/A to change accordingly. When the analog voltage at the output of the X D/A just passes the voltage input to the Cross-hair Generator from the X Position Pot, "X Coincidence" is reached, and the count once again switches to the Y Register. See Fig. 6-2 for illustration showing the generation of the Crosshair cursor.

Foldover. If the X Register begins counting to the right of the X Coincidence Point, the count continues to increment from the X Register until count 1023 is reached. When this occurs, the Most Significant Bit (MSB) of the X Register causes the Margin Shifter to output an End of Line ($\overline{\text{EOL}}$) signal. This signal is input to the Crosshair Generator to inhibit the count of the X Register. This delay allows the display beam time to return to the left side of the display and stabilize before the count resumes. This is known as Foldover (see Fig. 6-2). The signal from the Crosshair Generator (as a result of this action) is $\overline{\text{FPAUSE}}$. It inputs to the Format Effector to inhibit its functions during the time $\overline{\text{FPAUSE}}$ is active (0.5 ms). The count then continues

from 0 until X Coincidence is reached. When the count switches to the Y Register, the Crosshair Generator outputs $\overline{\text{DOWN}}$ pulses until the bottom of the page is reached. When this occurs, the beam folds over to the top of the page, but the Y Register continues to increment with no Foldover Pause. No Foldover Pause is needed in the Y Axis, because Foldover positions the beam off-screen. By the time the beam appears in the display area of the screen, it has had time to stabilize. The Y Register continues incrementing until coincidence again occurs; the X Register starts incrementing and the cycle repeats itself until commanded to do otherwise.

When the User sends the Header Character, Keyboard bits b1-b7 are inverted by the Multiplexer and placed onto the minibus lines as $\overline{\text{BIT 1}}$–$\overline{\text{BIT 7}}$. KSTROBE (which

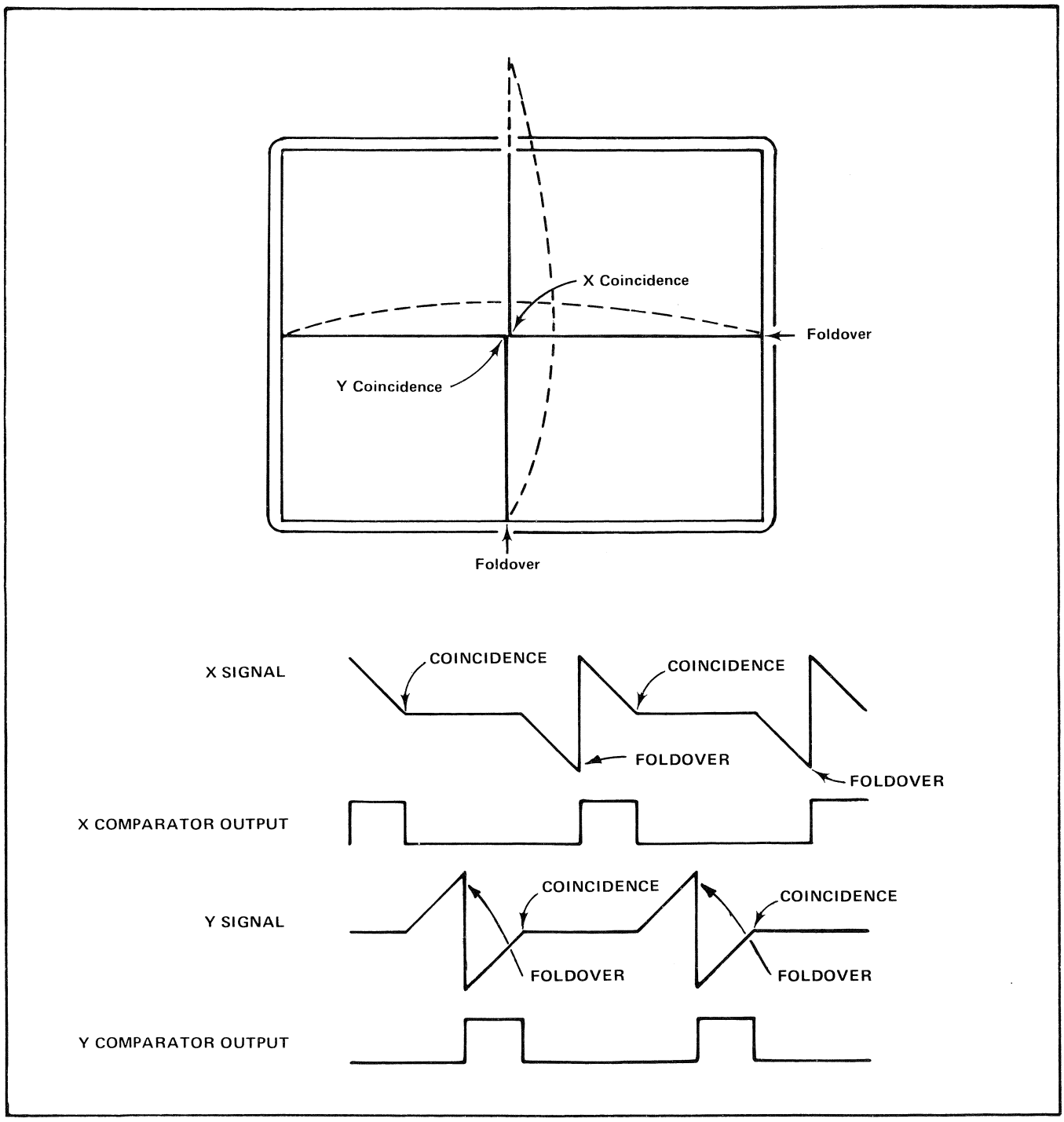


Fig. 6-2. Drawing a Crosshair Cursor Display.

accompanied the Keyboard bits) then generates the CSTROBE signal that strobes the data bits through the Interface card and to the computer. After the Header Character is accepted by the computer, the CBUSY line returns high, causing the GO DIGITIZE signal to go active. This causes the Crosshair Generator to stop the counting sequence when the next coincidence occurs. The digital representations of the voltages from the X and Y Position Pots are then held at the outputs of the X and Y Registers while the Crosshair Generator sends a PT FOUND signal back to the Multiplexer.

PT FOUND causes the Multiplexer to sample the five HIX bits from the X Register and place them along with code bits BIT 6 and BIT 7 on the minibus. Once again CSTROBE is generated and the HIX byte is sent to the computer. When CBUSY again goes inactive, the LOX bits are sampled by the Multiplexer and the process repeats, until all four coordinate bytes are sent to the computer. These may be followed by CR and/or EOT bytes if the circuit strap option is wired to do so.

The computer can request the coordinates of the crosshair by sending ESC plus SUB to initiate the GIN Mode as previously explained. Next, ESC plus ENQ is sent to set INQUIRE low. Upon the receipt of INQUIRE, the Multiplexer will send the coordinates of the intersection point to the computer as previously explained. However, in the place of the Keyboard character, the Multiplexer will send the Terminal Status Bits to the computer, MARG, NOLI, AUXSENSE, HCU, and GRAF.

The computer can also request the status of the Terminal by sending ESC plus ENQ. In this case, only INQUIRE is activated and the Terminal status bits plus the location of the display beam (lower left corner of the alpha cursor) are sent to the computer.

KEYBOARD DESCRIPTION

Refer to the Keyboard schematic. The Keyboard consists of the following principal circuits: an Oscillator, the 4 LSB Counter, the Character Decoder, the Character Detector, the 3 MSB Counter, the Bit 5 Control circuit, the Bit 7 Control circuit, and the Character Output Gates. Their combined purpose is to generate a coded character output on seven data lines labeled b1 through b7, and to develop a strobe output labeled KSTROBE to accompany the data bits.

Assume that characters are not being entered at the Keyboard. The Oscillator generates a symmetrical output pulse which is applied to Z9D, Z4, and Z7B. Z9D causes the 4 LSB Counter to continuously cycle through its 16 counts. Each time it completes a cycle, it feeds a pulse to a 3 MSB Counter, causing it to advance one. The 3 MSB Counter eventually cycles through its 8 counts and the entire performance is repeated. During this operation, the W output from the Character Detector holds a low on the Z4 gate. The pin 8 output of Z4 remains low, inhibiting outputs from the Character Output Gates.

When a character key is pressed, contact is made between an output of the Character Decoder and an input of the Character Detector. The output (ABC inputs) combination from the 3 MSB Counter into the Character Detector eventually reaches a code that selects the closed key. Since the 4 LSB Counter continues to cycle, a low is eventually placed on the closed key. This low is applied to the Character Detector, causing its W output to go high. This high provides enabling voltage to Strobe Generator Z4. When the Z13B output returns low, it causes a pulse of at least 7 milliseconds from the Strobe Generator. The 0 output from the Strobe Generator goes to Z9D to prevent additional clock pulses from affecting the 4 LSB Counter. At the same time, this low from the Strobe Generator goes to the Shift Latch and the Control Latch to gate through either the low or high from those devices as determined by the position of the Shift and/or Control keys.

The high from the 1 output of the Strobe Generator goes to the Character Output Gates, placing data on the b1 through b7 lines. When the Z13B output again goes low, it toggles Z7B, causing it to develop a high KSTROBE signal to strobe the data into the Terminal circuits.

The lows from Z13B are applied continuously to Z4, maintaining it in its one-set condition while the Keyboard key is held down. When the key is released, the high from the Character Detector is removed from Z4, permitting it to return to its zero-set state. This ends the b1-b7 output. The KSTROBE output ends on the next negative-going output of Z13B.

TC-1 BLOCK DIAGRAM DESCRIPTION

Introduction

The Operation of TC-1 can be best understood when it is broken down into three basic blocks of operation. These blocks are called Input/Decoding, Format Effector, and Character Generator. The three sections will be discussed in detail, beginning with the Input/Decoding section, then the Format Effector, then finally the Character Generator. Basically, the Input/Decoding Section decodes the various input signals and data for Terminal operations. The Format Effector Section is used to initiate a number of functions mainly associated with Alpha Mode. The Character Generator Section generates the alphanumeric characters and symbols.

Input/Decoding

General. Refer to the TC-1 Block Diagram and the TC-1 Schematic. The Input/Decoding Section contains the following circuits:

Home—When power is turned on, this circuit outputs the $\overline{\text{HOME}}$ signal that sets Terminal logic to Alpha Mode.

Column Decoder—Outputs signals that enable the Control Character Decoder, Character Generator, or Graphic Byte Decoder circuits.

Control Character Decoder—Decodes Control Characters used by the 4010.

Escape Flip-Flop—Used to prevent accidental activation of $\overline{\text{PAGE}}$, $\overline{\text{CURSE}}$, $\overline{\text{MAKE COPY}}$, and $\overline{\text{INQUIRE}}$ signals.

Page, Curse, Make Copy, and Inquire Circuits—Used in conjunction with Escape Flip-flop to prevent accidental activation of their respective outputs.

Graf Flip-flop—Sets Graphic Plot Mode.

Graphic Byte Decoder—Activated during Graphic Plot Mode to strobe coordinate address bytes into proper latch on TC-2.

Data Enable Gate—Strobes alphanumeric data into Character Generator.

Rubout Suppressor—Disables Data Enable Gate when DEL (Rubout) is received by the Terminal.

The description of the Input/Decoding Section will be given in that order. For the purpose of the description, assume that data is present on the minibus.

Home. Refer to the upper left corner of the Block Diagram. The purpose of this circuit is to reset all logic to the Alpha Mode when power is turned on (initialized). When power is turned on, the Home circuit applies a low pulse on the $\overline{\text{HOME}}$ line. If a Hard Copy Unit is connected to the 4010, this will prevent a copy from being generated due to voltage fluctuations that occur when power is initiated. Pulling the $\overline{\text{HOME}}$ line low resets Terminal logic to the Alpha Mode by inputting to the Graf Flip-flop (F/F) to set $\overline{\text{GRAF}}$ high and $\overline{\text{NOLI}}$ (No Linear Interpolation) low. $\overline{\text{HOME}}$ also resets the X and Y Registers (in TC-2) to position the writing beam to the Home position (upper-left corner of Display Screen). After the power stabilizes, the Home circuit is deactivated.

Column Decoder. Basically, the Column Decoder is a binary to decimal decoder. The inputs to the Column Decoder are as follows:

1. $\overline{\text{TERMINAL STROBE}}$ ($\overline{\text{TERM STB}}$) from U7B.
2. $\overline{\text{NOLI}}$ from Graf Flip-flop.
3. $\overline{\text{BIT 7}}$ from minibus.
4. $\overline{\text{BIT 6}}$ from minibus.

For any of the outputs from the Column Decoder to be active, $\overline{\text{TERM STB}}$ must be low. $\overline{\text{TERM STB}}$ goes low when $\overline{\text{TSTROBE}}$ is low, and when $\overline{\text{BTSUP}}$ and $\overline{\text{TSUP}}$ are high. This allows $\overline{\text{NOLI}}$, $\overline{\text{BIT 7}}$ and $\overline{\text{BIT 6}}$ to set the outputs.

Referring to the ASCII Code Chart in Fig. 6-3, notice that Columns 0 and 1 contain Control Characters; Columns 2 and 3 contain numerals and symbols; Columns 4 and 5 contain upper-case alpha characters and a few special symbols. Notice that $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ are the same for each group of two columns. The purpose of the Column Decoder, then, is to select these columns, two at a time. This is done by the distinct combinations of $\overline{\text{BIT 6}}$, $\overline{\text{BIT 7}}$, and $\overline{\text{NOLI}}$.

Refer to Fig. 6-4. In the Alpha Mode, the Column Decoder outputs an $\overline{\text{ALPHA STROBE}}$ signal that is used to enable the Character Latches through the Data Enable Gate. For $\overline{\text{ALPHA STROBE}}$ to become active, $\overline{\text{NOLI}}$ must be low, indicating that the Terminal is in Alpha Mode operation.

In the Alpha Mode, the only other output from the Column Decoder is the Control Character Strobe signal ($\overline{\text{CTRL CHAR STB}}$). For example, if $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ are both high, the Column Decoder will output the $\overline{\text{CRTL CHAR STB}}$ signal; thus providing an enabling voltage for the Control Character Decoder circuit. All other combina-

ASCII CODE FUNCTIONS

BITS B_4 B_3 B_2 B_1	B_7 B_6 B_5 = ø ø ø	ø ø 1	ø 1 ø	ø 1 1	1 ø ø	1 ø 1	1 1 ø	1 1 1
	CONTROL		HIGH X & Y GRAPHIC INPUT		LOW X		LOW Y	
ø ø ø ø	NUL ø	DLE 16	SP 32	ø 48	@ 64	P 8ø	\ 96	p 112
ø ø ø 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
ø ø 1 ø	STX 2	DC2 18	" 34	2 5ø	B 66	R 82	b 98	r 114
ø ø 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
ø 1 ø ø	EOT 4	DC4 2ø	$ 36	4 52	D 68	T 84	d 1øø	t 116
ø 1 ø 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 1ø1	u 117
ø 1 1 ø	ACK 6	SYN 22	& 38	6 54	F 7ø	V 86	f 1ø2	v 118
ø 1 1 1	BEL 7 BELL	ETB 23	' 39	7 55	G 71	W 87	g 1ø3	w 119
1 ø ø ø	BS 8 BACK SPACE	CAN 24	(4ø	8 56	H 72	X 88	h 1ø4	x 12ø
1 ø ø 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 1ø5	y 121
1 ø 1 ø	LF 1ø LINE FEED	SUB 26	* 42	: 58	J 74	Z 9ø	j 1ø6	z 122
1 ø 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 1ø7	{ 123
1 1 ø ø	FF 12	FS 28	, 44	< 6ø	L 76	\ 92	l 1ø8	¦ 124
1 1 ø 1	CR 13 RETURN	GS 29	- 45	= 61	M 77	] 93	m 1ø9	} 125
1 1 1 ø	SO 14	RS 3ø	. 46	> 62	N 78	^ 94	n 11ø	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	127 RUBOUT (DEL)

Fig. 6-3. ASCII Code Chart Illustration. The shaded characters show those that can not be transmitted with the TTY lock on.

tions of BIT 7 and BIT 6 will provide an ALPHA STROBE signal for the Data Enable Gate.

When the Graphic Plot Mode is set, NOLI goes high. No ALPHA STROBE will be generated. Instead, the combinations of BIT 7 and BIT 6 are decoded by the Column Decoder to generate code data to the Graphic Byte Decoder, and to generate CRTL CHAR STB. For an example, assume that BIT 7 and BIT 6 are 0-1, respectively. With TERM STB low and NOLI high, the Column Decoder will output code data to the Graphic Byte Decoder, which in turn sets LOXE low. If BIT 6 and BIT 7 both go high, the Column Decoder outputs the CTRL CHAR STB. Thus, no matter the mode of operation, the Column Decoder will always output the CTRL CHAR STB signal in response to highs on BIT 6 and BIT 7.

Control Character Decoder. The Control Character Decoder consists of two 4-line to 10-line decoders.

As a result of the enabling signals (CTRL CHAR STB and BIT 5) and the data (BITS 1–4), the Control Character Decoder will output low signals for the following Control Characters: US, BEL, VT, HT, BS, CR, LF, ENQ, GS, ESC, FF, SUB, ETB, SI, and SO. The Control Character signals are then processed by the applicable circuitry in TC-1 to perform the desired function.

Escape. Four Control Characters are dependent upon a preparatory command to arm the circuitry before they can be executed. The preparatory command is Escape (ESC) and the dependent commands are Form Feed (FF), which can be used to either exit the Terminal from Graphic Plot Mode or to initiate a PAGE (erase) signal; Substitute (SUB), which initiates the Graphic Input Mode and starts the Crosshair cursor; End of Tape Block (ETB), which activates the MAKE COPY pulse to turn on the Hard Copy Unit; and Inquire (ENQ), which is sent to request Terminal Status. The purpose of the Escape circuitry is to prevent accidental activation of these signals.

Assume that the ESC data bits are placed on the minibus. The Escape circuitry functions in the following manner. With BTSUP and TSUP inactive, TSTROBE (which accompanies the data bits) enables the Column Decoder to generate the CTRL CHAR STB signal. This signal permits the Control Character Decoder to decode BIT 1–BIT 5; the ESC signal goes active and "arms" the Escape Flip-flop, setting LCE (Last Character to Escape) high. The arrival of the data bits for the next portion of the two-character sequence activates the required function. ETB will activate MAKE COPY; FF will activate PAGE; SUB will activate CURSE; and ENQ will activate INQUIRE. LCE will return low when the next TSTROBE pulse ends following the escape sequence. The positive-going CLEAR signal from U8A (which occurs whenever TSTROBE ends) disarms the Escape F/F unless the ESC character accompanies TSTROBE. Thus, the Escape FF is always disarmed by the character following the ESC input, regardless of whether it was FF, ETB, SUB, ENQ, or some other character.

Page-Curse-Make Copy-Inquire. These four circuits comprise an additional portion of the Escape circuitry. The Page circuit is composed of a simple logic circuit. LCE must be high and FF must be low to activate the PAGE signal. PAGE is used to erase the display and to also pulse the

INPUT SIGNAL					
TERM STB	NOLI	BIT7	BIT6	RESULTANT SIGNAL	COLUMNS OF ASCII CODE CHART
0	0	0	0	ALPHA STB	6 and 7 (LOW CASE)
0	0	0	1	ALPHA STB	4 and 5 (UPPER CASE)
0	0	1	0	ALPHA STB	2 and 3 (SYMBOLS & NUMERALS)
0	0	1	1	CTRL CHAR STB	0 and 1 (CTRL CHARACTERS)
0	1	0	0	LOY	6 and 7 (5 LSB or Y ADDRESS)
0	1	0	1	LOXE	4 and 5 (5 LSB of X ADDRESS)
0	1	1	0	HIY HIX	2 and 3 (5 MSB of Y ADDRESS)* 2 and 3 (5 MSB of X ADDRESS)*
0	1	1	1	CTRL CHAR STB	0 and 1 (CTRL CHARACTERS)

*Preceding signal determines whether HIY or HIX goes active.

*HIY goes active following a GS or the LOXE signal; HIX goes active following the LOY signal.

Fig. 6-4. Logic Table for Column Decoder and Graphic Byte Decoder.

4010 out of Graphic operation. The Curse circuit is also composed of a simple logic circuit. LCE must be high and SUB must be low in order to activate the CURSE signal. CURSE is used to switch the Terminal into the Graphic Input Mode by activating the Crosshair Generator in TC-2. The Make Copy circuit must have LCE high and ETB low in order to activate the MAKE COPY pulse. The 600 Hz input from the Alpha Cursor Counter is used to develop a MAKE COPY pulse of the desired width. HOME inhibits the Make Copy circuit when power is turned on. Notice that MAKE COPY inputs to the Terminal Busy circuit. This keeps the Terminal Busy (TBUSY goes low) until the Hard Copy Unit asserts DRBUSY to sustain the busy condition. This holds the 4010 in a busy condition from the time MAKE COPY is activated to the time the Hard Copy Unit completes the copy (DRBUSY goes high).

Graf Flip-flop (F/F). The Graf F/F is used to switch the Terminal in and out of the Graphic Plot Mode. The GS Control Character sets the Graphic Plot Mode. NOLI goes high to enable the Linear Interpolation circuitry in TC-2. GRAF goes low and is used to set other Terminal circuitry for Graphic Plot operation. The signals PAGE, CURSE, HOME, will reset the Graf F/F to the Alpha Mode. The Control Characters US and CR can also reset the Graf F/F to the Alpha Mode.

When GS sets GRAF low and NOLI high, NOLI enables the Column Decoder to allow BIT 7 and BIT 6 to control the Byte Enable lines to the Graphic Byte decoder.

Graphic Byte Decoder. This circuit is used to generate the graphic byte output signals HIY, LOY, HIX, and LOXE. These signals are used to load the four graphic bytes into the Data latches on TC-2. When the 4010 receives graphic plot data, it arrives in a sequence of four, seven-bit bytes for each coordinate point addressed. Five of the bits contain coordinate information and 2 of the bits (bits 6 and 7) contain steering data. The steering data designates the specific byte as being either High Order Y (HIY), Low Order Y (LOY), High Order X (HIX) or Low Order X (LOX). For the sake of this discussion we will assume that data is being received in that order. (For other graphic byte sequences, see the 4010/4010-1 User's Manual.) The Graphic Byte Decoder operates in the following manner.

When the 4010 receives a GS Control Character, it activates the GS signal from the Control Character Decoder. This signal sets the Graphic Plot Mode as previously explained. With NOLI inactive (high), the Column Decoder will now interpret BIT 6 and BIT 7 as BYTE ENABLE information for the Graphic Byte Decoder. The Graphic byte code bits are as follows:

BYTE	BIT 7	BIT 6	
HIY	0	1	Most significant 5 bits of Y
LOY	1	1	Least significant 5 bits of Y
HIX	0	1	Most significant 5 bits of X
LOX	1	0	Least significant 5 bits of X

Notice that the HIY and HIX bits have the same bit 7 and bit 6 configuration. The problem of interpreting which byte is which is accomplished by the GS signal and the LOX byte. On the first vector string, the GS signal (through U5F) sets the Graphic Byte Decoder to interpret the first high order code as being HIY; thus, the HIY signal is activated. The Graphic Byte Decoder interprets the next high order code as being HIX; subsequently the HIX signal is activated. On succeeding vector strings, the LOX code sets the Graphic Byte Decoder to interpret the following high order code as being HIY.

Notice that the GIN signal inputs to the Graphic Byte Decoder. Its purpose is to inhibit the Decoder during the sending of graphic input data to the computer.

Data Enable Gate. This circuit puts out an ENABLE signal to the Character Generator circuitry whenever ALPHA STROBE and DELETE are both low. The ENABLE signal then latches the data bits into the Character Generator.

Rubout Suppressor. The main purpose of this circuit is to suppress the data code 127 (DEL). The Character Generator will neither space nor print because the Rubout Suppressor circuit detects the DEL code and sends a high DELETE signal to the Data Enable Gate. This action prevents the ALPHA STROBE signal from generating an ENABLE signal, thus inhibiting the Character Latches. This prevents the DEL code bits from being input to the Character Generator.

Format Effector

General. The Format Effector operates from a predetermined set of inputs to position the alpha (pulsating) cursor over the face of the display screen. It will also generate timing pauses when switching out of Graphics, when initiating a Carriage Return, when ringing the bell, and when drawing a vector.

Its basic function is to take the decoded output of the Control Character Decoder and transform it into the desired result. For example, if the function desired is to move the alpha cursor one space, the Format Effector will output 22 pulses on the RIGHT line. This will increment

the X Register in TC-2, thus moving the alpha cursor one space. Each pulse will increment the X Register one count. Each count from the Register will move the Display beam one Tekpoint. A Tekpoint refers to one of the 1024 programmable locations that are available in both the X and Y Axes. Another example is a Carriage Return. With a Carriage Return, the Control Character Decoder outputs the $\overline{CR}$ signal. The Format effector circuitry inverts the $\overline{CR}$ to CR, which sets the X Register back to zero. At the same time, the Format Effector generates a pause in Terminal operation, causing the Terminal to go to a "busy" condition. This pause is of sufficient length to allow the display beam to position back to the left side of the screen before the Terminal will accept and process further data.

The Format Effector contains the following circuits:

System Clock—Provides timing signals for Terminal operation.

Alpha Cursor Counter—Controls the positioning of the alpha cursor as well as various other functions.

Pulse Shaper—Provides a pulse that loads preset data into the Alpha Cursor Counter circuit.

Direction Latch—Remembers the direction of last alpha cursor movement. Its output changes when new direction command is received.

Direction Enable Gates—Enables $\overline{LEFT}$, $\overline{RIGHT}$, $\overline{UP}$, or $\overline{DOWN}$ lines dependent upon respective signals from Direction Latches and the enabling signals from the Alpha Cursor Counter.

Terminal Busy—Outputs a $\overline{TBUSY}$ signal that prevents the Terminal from receiving any further data until the Terminal operation being performed is completed.

Auto Carriage Return/Line Feed (Auto CR/LF)—Performs an automatic Carriage Return with the receipt of the LF Control Character. Processes the CR signal to activate a Carriage Return.

Vector/Bell Enable—Outputs signals that activate vector drawing and bell ringing.

Z Axis—Controls the state of the X signal that turns the display beam on and off.

Bell—Provides the drive signal for the speaker that gives the audible "bell" tone.

View/Hold—Provides an enabling signal (VIEW) for the CRT flood guns so that data can be viewed. When in Hold operation, VIEW is set at a reduced duty factor, thus prolonging the life of the CRT.

Cursor Refresher—Provides logic that allows the 5 X 7 dot matrix of the Character Generator to be displayed but not stored, thus generating the alpha cursor.

Defocus—Provides uniform focusing in Alpha Mode. In Graphic operation it allows the display beam to become slightly defocused so that the vectors will not appear as a series of dots.

Basically, the operation of the circuits will be described in that order. However, in some cases it is more practical to combine the descriptions of several blocks.

Block Description

System Clock. The System Clock is a Crystal Controlled oscillator that outputs two square wave frequencies to the minibus—4.9 MHz and 614 kHz. It also outputs a 2.45 MHz square wave for use by the Alpha Cursor Counter and the Auto CR/LF circuits.

Pulse Shaper. The Pulse Shaper generates a $\overline{LOAD}$ pulse that is used to strobe data from the preset lines into the Alpha Cursor Counter. The $\overline{LOAD}$ pulse is shorter than any of the inputs to the Pulse Shaper Circuit. This allows the $\overline{LOAD}$ pulse to come and go while the data on the preset lines is still valid. All inputs to the Pulse Shaper will activate the $\overline{LOAD}$ pulse. The $\overline{LOAD}$ pulse is inverted and inputs to the Vector/Bell Enable and Direction Latch circuits as a LOAD signal.

Alpha Cursor Counter, Direction Latch, and Direction Enable Gates. The Alpha Cursor Counter is composed of 4, four-bit counter elements. Depending upon preset inputs to the counter, it will add or subtract the required number of pulses to initiate the function required by the Control Character Decoder. This circuit also generates pauses in Terminal operation; such as that required for a Carriage Return, (as previously explained), and coming out of Graphics operation. It also provides a 2.6 ms pause that activates the $\overline{Z}$ signal when drawing a vector. Finally, it provides various timing signals that are used by other TC-1 circuits.

The Clock input to the Alpha Cursor Counter is a 2.45 MHz square-wave from the System Clock. The Counter counts continuously except when a low is applied on the $\overline{LOAD}$ input line. As the Counter circuitry is counting it is putting out the following square wave signals for use by other TC-1 circuits.

5 Hz and 37 Hz. Used in the Cursor Refresher Circuit

75 Hz, 150 Hz, 300 Hz. Used in the View/Hold Circuit.

600 Hz. Used in the Make Copy Circuit.

1200 Hz. Used in the Bell Circuit.

19 kHz and 77 kHz. Used by the Character Generator.

1.25 MHz. Used to increment the Direction Enable Gates and to clear the Column reset circuitry located in the Character Generator circuitry.

Basically, the Alpha Cursor Counter is a programmable counter, referred to as such because it contains a number of preset (program) lines that "program" the Alpha Cursor Counter to output various signals that perform a specific function. The data loaded into the Counter from the preset lines determines a number that the Counter will start counting from. These preset inputs are, $\overline{\text{LOXE}}$ (Low Order X) which sets the 2.6 ms pause that activates the Z signal to draw a vector; the Bell inputs that determine how long the bell will ring; The $\overline{\text{CR}}$ input that initiates the pause needed to perform the Carriage Return; and finally BS (Backspace), $\overline{\text{HT}}$ (Horizontal Tab), $\overline{\text{VT}}$ (Vertical Tab) and $\overline{\text{LF}}$ (Line Feed). (Notice that the same preset line is used for both directions of horizontal movement; similarly, one preset line is used for both directions of vertical movement. This is because that for either a BS or an HT, the horizontal movement is 14 Tekpoints. For either a VT or an LF, the vertical movement is 22 Tekpoints.) Each of the eight functions that the Counter will perform corresponds to a definite value on the preset input lines. These lines determine how long it will take for the Counter to count up to the point where a zero-to-one transition is obtained on its Most Significant Bit (MSB) output. If either a LEFT, RIGHT, UP, or DOWN signal is being output by the Direction Latch, this length of time determines how many 1.25 MHz pulses are placed on the $\overline{\text{LEFT}}$, $\overline{\text{RIGHT}}$, $\overline{\text{UP}}$, or $\overline{\text{DOWN}}$ line, as well as how long $\overline{\text{TBUSY}}$ stays active. In all cases, the MSB signal being low determines how long it will take for a Terminal pause, as reflected by the $\overline{\text{TBUSY}}$ signal.

For an over-all example of how the Format Effector processes a direction command, assume that the Control Character HT (space) has been received by the Terminal. $\overline{\text{HT}}$ inputs to the Pulse Shaper circuit and causes the $\overline{\text{LOAD}}$ pulse to go low. LOAD then strobes the $\overline{\text{HT}}$ signal into the Direction Latch, activating the RIGHT signal; $\overline{\text{LOAD}}$ simultaneously loads the preset data into the Alpha Cursor Counter causing the MSB signal to go low. With MSB low, $\overline{\text{TBUSY}}$ goes active and the 1.25 MHz signal can clock the Direction Enable Gates. With the RIGHT signal from the Direction Latch high, every time the 1.25 MHz signal goes low, a low-going transition takes place on the $\overline{\text{RIGHT}}$ line, incrementing the X Register in TC-2. After 14 positive-to-negative transitions of the 1.25 MHz signal, the MSB signal will go high. This prevents the 1.25 MHz signal from enabling further $\overline{\text{RIGHT}}$ pulses. It also ends the $\overline{\text{TBUSY}}$ signal.

The $\overline{\text{FPAUSE}}$ signal is an output of TC-2. Its purpose is to disable the Alpha Cursor Counter circuit when the X Register in TC-2 resets from 1023 back to 0. Here it is used to generate the pause required for proper operation of the Auto Carriage Return Line Feed circuit when used with a clocked interface. It does not cause the MSB signal to go low. It simply stops the counting sequence for approximately 0.5 ms.

Terminal Busy. The purpose of the Terminal Busy circuit is to inhibit the reception of data from either the Keyboard or the computer. Any of the following functions will cause $\overline{\text{TBUSY}}$ to go active low; when an alphanumeric character is being generated ($\overline{\text{CHAR IN PROG}}$); when a Hard Copy is being generated ($\overline{\text{MAKE COPY}}$ and $\overline{\text{DRBUSY}}$); and when the Most Significant Bit (MSB) output of the Alpha Cursor Counter is low (as is the case when it is performing one of the eight functions).

Automatic Carriage Return/Line Feed. When the Control Character Decoder outputs an $\overline{\text{LF}}$ signal, the Auto CR/LF circuit will in turn output an $\overline{\text{LF}}$ signal to the Pulse Shaper and Direction Latch circuits to cause the Line Feed to occur. Notice that the Control Character signal $\overline{\text{CR}}$ also inputs to this circuit. This signal is inverted and outputs on the CR line. The Auto CR/LF circuit can be strapped (see Strappable Options Section of the Manual) to give an automatic Carriage Return when $\overline{\text{LF}}$ goes active. If the strap is in place for an automatic Carriage Return with Line Feed, $\overline{\text{LF}}$ also generates the CR signal.

The $\overline{\text{EOL}}$ (End of Line) input (from TC-2) activates an automatic Carriage Return and Line Feed when spacing past the right margin. An active SUPPRESS signal from the Alpha Cursor Suppress circuit inhibits the operation of the automatic CR/LF circuit.

Vector/Bell Enable. When the Control Character $\overline{\text{BEL}}$ goes low, it enters the Pulse Shaper to generate the $\overline{\text{LOAD}}$ pulse. $\overline{\text{BEL}}$ then gets strobed into the Vector/Bell Enable circuit by the LOAD pulse. The circuit then outputs BELL and $\overline{\text{BELL}}$ to generate the Bell tone. For more on how the Bell Circuit works, see the explanation on the Bell Circuit. This circuit is also used to enable or disable the Z axis during the drawing of a vector (Linear Interpolation). It functions in the following manner.

Circuitry within the Vector/Bell Enable circuit keeps the VECTOR ENABLE signal to U73B low for the first vector following GS. This is known as a "Dark Vector". With the receipt of the next vector, the $\overline{\text{LOXE}}$ signal, causes the Vector/Bell Enable circuit to set the VECTOR ENABLE signal high. VECTOR ENABLE provides an enabling voltage to one side of the Vector Enable Gate U73B. The $\overline{\text{LOXE}}$ signal also inputs to the Alpha Cursor Counter to

preset the inputs for a 2.6 ms pause. The $\overline{\text{LOAD}}$ signal then sets the 2.6 ms PAUSE line to U73B high. U73B is now enabled and sends a low $\overline{\text{DRAW}}$ signal to the Z Axis Circuit. This action sets the $\overline{\text{Z}}$ signal low to draw the vector. 2.6 ms later, the 2.6 ms PAUSE line goes low, disabling the Z Axis Circuit.

Z Axis. The Z Axis circuitry is used to enable or disable the $\overline{\text{Z}}$ signal. $\overline{\text{Z}}$ is an active low signal that is used to turn the writing beam on. The effect that $\overline{\text{DRAW}}$, $\overline{\text{TOP ROW SUPPRESS}}$, $\overline{\text{WRITE DOT}}$, and REFRESH have upon Z Axis operation is described in the block from which they originate.

Bell. When the Control Character BEL is received, $\overline{\text{BEL}}$ goes low from the Control Character Decoder. $\overline{\text{BEL}}$ inputs to the Pulse Shaper circuit to generate a $\overline{\text{LOAD}}$ pulse that is inverted to latch $\overline{\text{BEL}}$ into the Vector/Bell Enable Circuit. This causes the Bell and $\overline{\text{BELL}}$ signals to go low and high respectively. While the $\overline{\text{LOAD}}$ pulse is active low, it latches the BELL and $\overline{\text{BELL}}$ inputs into the Alpha Cursor Counter and the Counter starts counting. The $\overline{\text{LOAD}}$ pulse also causes the MSB output of the Counter to go low. This low MSB signal with the high $\overline{\text{BELL}}$ signal from the Vector/Bell Enable circuit allows the 1200 Hz square wave signal to drive the Bell circuit, thus generating the 1200 Hz tone. When the Counter counts up to the point where the MSB goes high (as determined by the preset input from the Vector/Bell Enable circuit) the Bell circuit is disabled.

View/Hold. The purpose of the View/Hold Circuit is to prolong the life of the display tube. In the Alpha Mode, as long as data is being entered into the Terminal, the VIEW signal is high, allowing data to be displayed. However, if no new data is entered for a period of about 90 seconds the VIEW signal becomes driven by a 75 Hz signal from the Alpha Cursor Counter. This action provides a 12 1/2% duty time for the VIEW signal, thus dimming the display. This is known as "Hold" Mode. The display can be returned to normal viewing level by entering new data.

For the above action to take place, the input signals must be in the following states:

1. SUPPRESS—Low
2. $\overline{\text{HOME}}$—High
3. $\overline{\text{SHIFT}}$—High
4. $\overline{\text{RESET/SUPPRESS}}$—High

Notice also that this circuit inputs a signal called $\overline{\text{VIEW}}$ to the Cursor Refresher Circuit. When the 90 second period occurs, this signal goes low to inhibit the Alpha Cursor during the time the Terminal is in hold.

If either the $\overline{\text{GRAF}}$, $\overline{\text{GIN}}$, $\overline{\text{DRBUSY}}$ or $\overline{\text{TERM STB}}$ signals go active, the SUPPRESS signal from the Alpha Cursor Suppress circuit goes high. This keeps the view signal active.

Cursor Refresher. The Alpha Cursor is a pulsating display of the 5 X 7 dot matrix within the Character Generator. When the Terminal is in the Alpha Mode and no new data is being entered, the Character Generator will cycle through the dot matrix 75 times each second (for explanation on how the characters are generated, see the Character Generator Description). Each time a dot of the matrix is to be displayed, the $\overline{\text{WRITE DOT}}$ signal from the Character Generator will go low to enable the Z Axis circuit. The $\overline{77\text{ kHz}}$ signal is input to the Cursor Refresher Circuit, causing the REFRESH line to go high. This causes $\overline{\text{Z}}$ to blank between dots. However, under these circumstances the Matrix will store, because the Z Axis Circuit has no way of knowing whether a character is being generated or the Character Generator is just cycling through the matrix. Therefore, the width of the $\overline{\text{Z}}$ pulse must be limited to prevent storing of the Alpha Cursor when no characters are being generated. This is the purpose of the Cursor Refresher. Not only does it prevent the character Matrix from storing, but it also causes the Matrix to "blink", thereby drawing the User's attention to the location of the writing beam.

A 5 Hz square wave is placed at the input to the Cursor Refresher Circuit. The 37.5 Hz square wave, and the CARRY signal (from the Column Counter in the Character Generator) combine to give a short pulse that fires a one-shot multi in the Cursor Refresher circuit. The on time of this multi is only 0.75 ms. But, in this span of time, the Character Generator is permitted to scan completely through the matrix, once. Referring to Fig. 6-5 you will notice a drawing of the composite signal as viewed on the REFRESH and $\overline{\text{Z}}$ lines when the multi is on. Notice that there are five sequences of 8 pulses each. Each of these pulses corresponds to one dot in the matrix; each set of eight pulses corresponds to one column of the matrix; the five sequences of pulses corresponds to the entire matrix. Note, however, that when viewing the $\overline{\text{Z}}$ signal, the eighth pulse for each column is missing. This is because the top (eighth) row of the matrix is inhibited by the $\overline{\text{TOP ROW SUPPRESS}}$ signal to the Z Axis circuit. This gives us the 5 X 7 matrix. Notice also the space between columns. This span of time is caused by the $\overline{\text{RESET/SUPPRESS}}$ signal that originates in the Top of Column Pause circuit of the Character Generator. Each time the count switches to another column, the display beam needs sufficient time to settle down before the count can continue; hence, the pause at the top of each column.

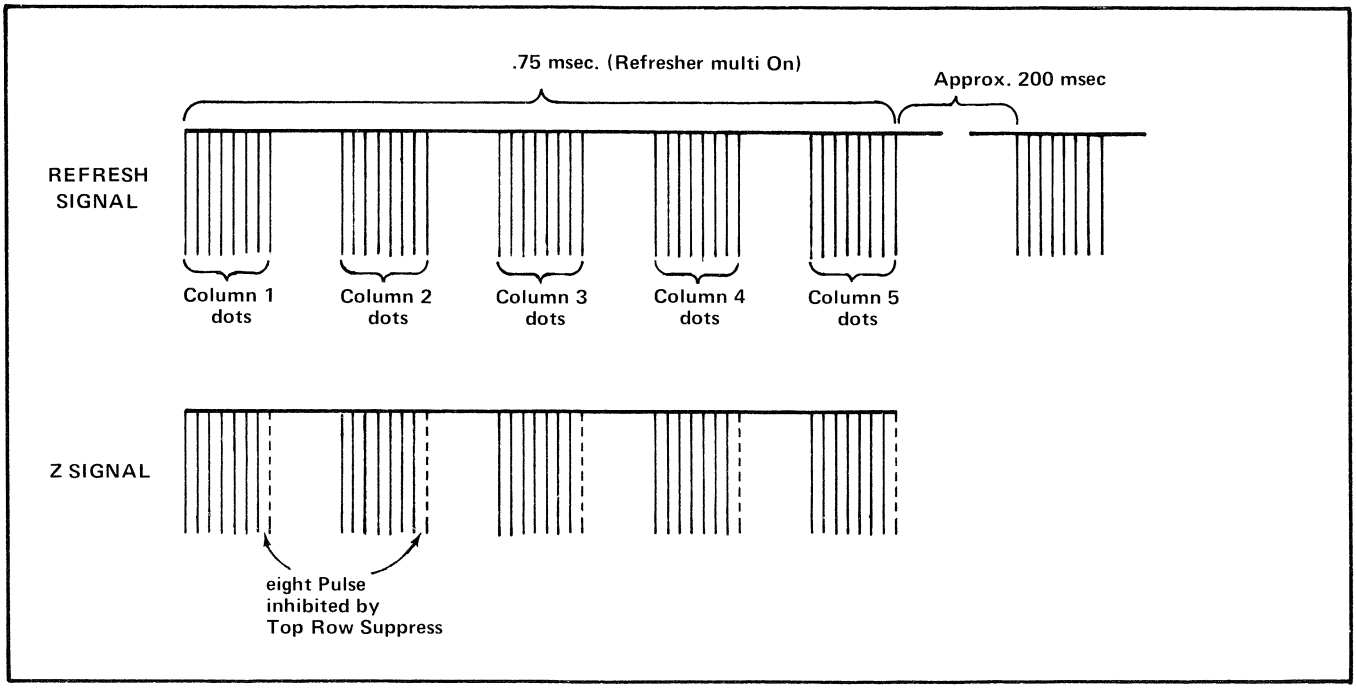


Fig. 6-5. Illustration of Refresh and Z signals During Generation of the Alpha Cursor.

The above-stated action occurs approximately five times each second. The blinking of the pulsating Alpha Cursor is the result of this 5 Hertz repetition rate. The whole process has combined to give a signal of short enough pulse width so as not to store the matrix on the screen.

The $\overline{\text{VIEW}}$ signal inputs to the Cursor Refresher circuit to inhibit the Alpha Cursor when the View/Hold circuit sets the Terminal to the Hold Mode. The $\overline{\text{VIEW}}$ signal must be low to inhibit the Alpha Cursor. The $\overline{\text{TERM STB}}$ input from U7B will inhibit the cursor Refresh circuit while $\overline{\text{TSTROBE}}$ is active.

Defocus. The Defocus circuit is used to generate the $\overline{\text{FUZZ}}$ signal. $\overline{\text{FUZZ}}$ is low in Alpha Mode to provide uniform focusing. It goes high during graphic operation to slightly defocus the display beam.

Character Generator

General. The Character Generator performs its function by cycling through a rectangular dot matrix. See Fig. 6-6. Although the matrix is formed by the coordinates of eight rows and five columns, the eighth (or upper) row is always blanked during character writing.

Characters are formed by cycling through each of the matrix positions and writing a dot in each of the positions required for forming a character. Cycling sequence consists of selecting column one, rippling through rows 8 through 1, then selecting column 2, repeating the row selection, etc. For example, if the letter L were to be written, dots would be written for each row position in column 1. Only the row 1 dots would be written when the character generator cycles through the eight rows of the remaining four columns.

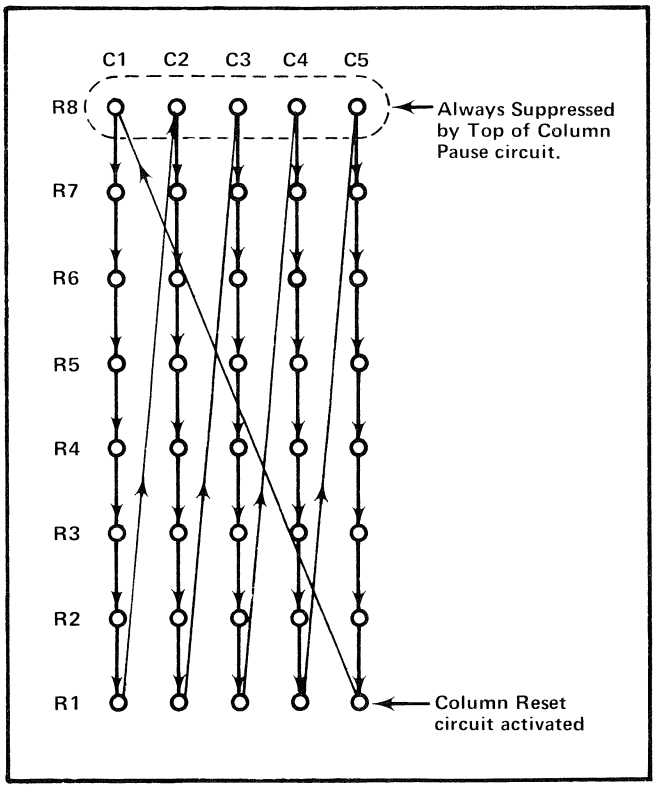


Fig. 6-6. Character Generator Matrix.

In the absence of a character input, the Character Generator continuously cycles through the matrix, writing all dots in rows 7 through 1, forming a non-storing cursor. When a character is ordered written, the matrix is scanned, dots are written to store the character, and then a pulse is sent to the Format Effector to advance the X Register one character position to prepare for the next character.

The principal circuits which perform these functions within the Character Generator are as follows:

Read Only Memory (ROM)—Programmed by the character being processed; emits each of eight sets of data on five parallel lines, the set being determined by the Row Counter; the five parallel lines represent the five columns of the character writing matrix. The ROM has 64-character selection capability. This consists of the middle four columns of the ASCII Code Chart. None of the lower case alphanumeric symbols can be generated; although eliminating character $\overline{\text{BIT 6}}$ from the ROM permits characters from the right two columns of the ASCII Code Chart to be accepted and written as characters from an equivalent position in the two columns to the left.

Column Counter—sequentially selects columns one through five, causing the CRT beam to deflect in the X direction; selects the appropriate column out of the five outputs of the ROM for Z axis control.

Row Counter—cycles through the eight rows at each column selection; its output causes the CRT beam to deflect in the Y direction; it also causes the ROM to emit five bits of writing information consistent with the selected row.

Z Multiplexer—emits an output controlled by one of the five signals from the ROM. The selection is controlled by the inputs from the Column Decoder.

Additional circuits instrumental to the Character Generator operation are:

Alpha Cursor Suppress—prevents operation during graphics modes, during hard copy writing, etc.

ROM Selector—selects ROM A or ROM B (if ROM B is installed).

Character Latches—loads character bits into the Character Generator with the receipt of an active ENABLE signal.

Character Status—activates the generation of a character. Sets $\overline{\text{TBUSY}}$ active; completes the character generation process by sending a signal to the Format Effector to space to the next character position.

Z Enable Gate—sends 77 kHz $\overline{\text{Z ENABLE}}$ pulses to the Z Multiplexer.

Y Matrix Digital to Analog—converts the digital output of the Row Counter into its analog equivalent for display beam positioning. Also sends a $\overline{\text{TOP ROW SUPPRESS}}$ signal to the Z Axis circuit that suppresses the eighth row of dots.

X Matrix Digital to Analog—converts the digital output of the Column Counter into its equivalent analog voltage for display beam positioning.

Top of Column Pause—provides a pause in the scanning sequence to allow the display beam time to position to the top of the matrix and stabilize.

Column Reset—resets the Column Counter to column 1.

Terminal Strobe ($\overline{\text{TERM STB}}$) signal—presets the outputs of the Character Generator circuitry so as to be in position to begin displaying a character immediately when commanded.

Echoplex Suppressor—inhibits character generation.

Selecting the ROM. Refer to the TC-1 Block Diagram. The standard 4010 is provided with one Read Only Memory circuit; however, space is provided on TC-1 for an additional Read Only Memory device. The selection of the Read Only Memory device is controlled by the output of the Read Only Memory Selector Circuit. The ROM chips are connected in parallel, with the exceptions of the ROM Select line. Under normal operation ROM A will be selected. The alternate, ROM B is selected by pressing Switch 2 on the Front Panel or by sending Control Character SO. ROM A is selected by sending Control Character SI, by pressing the Reset key, or when power is turned which activates the $\overline{\text{HOME}}$ signal.

Presetting the Character Generator. When the data bits for an alphanumeric character are received by the Terminal, $\overline{\text{TSTROBE}}$ activates the $\overline{\text{TERM STB}}$ signal. $\overline{\text{TERM STB}}$ going active causes the Column Reset circuit to output a COLUMN RESET pulse that resets the Column Counter to Column 1. $\overline{\text{TERM STB}}$ also inputs to the Alpha Cursor Suppress circuit, causing it to activate the SUPPRESS signal. This signal inputs to the Top of Column Pause circuit, the Row Counter circuit, and the Y Matrix Digital to Analog circuit, causing these circuits to inhibit the scanning sequence that had been drawing the non-storing pulsating cursor. The Row Counter outputs are all set low. This represents the Row 8 position of the character matrix. Even though the low Row Counter inputs to the Y Matrix Digital to Analog signify the Row 8 position, the output of the Y Matrix Digital to Analog is held at the Row 1 position of the character matrix by the active SUPPRESS signal. When $\overline{\text{TSTROBE}}$ goes inactive, SUPPRESS also goes

inactive, allowing the low outputs of the Row Counter to set the output of the Y Matrix Digital to Analog circuit to the Row 8 position. The sequence in which $\overline{\text{TSTROBE}}$ goes inactive will be explained in more detail in the "Scanning the Character Matrix" description.

SUPPRESS also goes active when operating in Graphic Plot and Gin modes or when the Hard Copy Unit is making a copy of the displayed data. During the operation of these modes, the SUPPRESS signal holds the display beam in the Row 1, Column 1 position of the character matrix.

When $\overline{\text{TERM STB}}$ causes the $\overline{\text{ALPHA STB}}$ signal to go active, the data bits ($\overline{\text{BIT 1}}$–$\overline{\text{BIT 5}}$ and $\overline{\text{BIT 7}}$) that contain the alphanumeric character are strobed through the Character Latches by the ENABLE signal (the DELETE signal from the Rubout Suppressor must be inactive). The Character bits then select the address of the character within the ROM device.

The ENABLE signal also activates the $\overline{\text{CHAR IN PROG}}$ signal from the Character Status circuit. This signal inputs to the Terminal Busy circuit to hold $\overline{\text{TBUSY}}$ active until the Character Generator has completed drawing the Character. The complement of the $\overline{\text{CHAR IN PROG}}$ signal enables the Z Enable Gate, allowing it to pulse the Z Multiplexer with 77 kHz square wave signals.

Scanning the Character Matrix. $\overline{\text{BIT 1}}$–$\overline{\text{BIT 5}}$ and $\overline{\text{BIT 7}}$ applied to the data inputs of the ROM select the writing signals pertaining to the character being input. The BCD, ROW, inputs from the Row Counter, sequentially scan the matrix rows in the ROM at a 77 kHz rate. The combination of data select and Row scanning inputs results in dot disclosure information on the five output lines of the ROM to the Z Multiplexer circuit. The five lines represent each of the five columns of the matrix. With this information in mind, let's follow the Character Generator through the scanning sequence.

When the $\overline{\text{TSTROBE}}$ signal ends, $\overline{\text{TERM STB}}$ goes inactive, causing the SUPPRESS signal from the Alpha Cursor Suppress circuit to go inactive. SUPPRESS going inactive allows the output of the Y Matrix Digital to Analog circuit to set the Display beam to the row 8, column 1 position of the matrix. The eighth row of dots is not used; therefore, a $\overline{\text{TOP ROW SUPPRESS}}$ signal is sent to the Z Axis circuit to inhibit the $\overline{\text{Z}}$ signal. SUPPRESS going inactive also enables the Row Counter. With the first 77 kHz signal, the Row Counter will advance to the row 7 position. This causes the ROM device to send all 5 dots of row 7 information to the Z Multiplexer. However, because the Column Counter output signifies that column 1 is being counted, it sets the Z Multiplexer to look at the COLUMN 1 DOT inputs from the ROM. If the ROM signifies that the dot is to be written, the COLUMN 1 DOT output is high. When the 77 kHz signal causes the $\overline{\text{Z ENABLE}}$ to go low, the output of the Z Multiplexer ($\overline{\text{WRITE DOT}}$) also goes low to cause the Z Axis circuit to output a $\overline{\text{Z}}$ signal to write the dot.

The above process repeats itself; the 77 kHz pulses cause the Row Counter to count from 1 to 7, selecting row 7 to row 1 respectively; with each advance of the Row counter the Y Matrix Digital to Analog will change accordingly, positioning the display beam to follow the scanning sequence.

When the Row Counter resets state 0, the state 4 goes low. This causes the Column Counter output to advance to column 2. The output of the X Digital to Analog circuit changes and positions the display beam to the column 2 position. Resetting the Row Counter to state 0 once again causes the $\overline{\text{TOP ROW SUPPRESS}}$ signal from the Y Matrix to go active, but, the counting sequence cannot continue because the state 4 line going low activated the Top of column Pause circuit, inhibiting the 77 kHz pulses that clock the Row Counter. The Top of Column Pause circuit provides a 60 μs delay in the counting sequence to allow the display beam time to deflect to the row 8 position and stabilize. The 19 kHz signal input from the Alpha Cursor Counter ends the delay and the scanning sequence continues in the described manner; except that this time the output of the Column Counter has set the Z Multiplexer to output dot information from the COLUMN 2 DOTS output of the ROM. The above sequence repeats until all five columns of the Character matrix have been scanned. It takes about 700 microseconds to scan the character matrix once.

Resetting the Character Generator. When the Row Counter resets to state 0 when counting past Row 1, Column 5 (see Fig. 6-6), the low-going most significant bit of the Row Counter again causes the Top of Column pause circuit to generate the 60 μs pause. It also causes the Column Counter to activate the CARRY signal. (The CARRY signal actually signifies a count of five from the Column Counter.) The CARRY signal inputs to the Top of Column Pause circuit to generate the $\overline{\text{RESET/SUPPRESS}}$ signal that activates the COLUMN RESET signal from the Column Reset circuit. The COLUMN RESET signal resets the Column Counter back to Column 1.

When the CARRY signal went active it caused a CHAR COMP signal to be sent from the Character Status circuit to the Pulse Shaper circuit. This signal causes the Format Effector circuitry to advance the display beam one character space. On the trailing edge of the CARRY signal (caused by the COLUMN RESET signal resetting the Column Counter to Column 1), the $\overline{\text{CHAR IN PROG}}$ signal (that is holding the Terminal busy) ends. The CHAR COMP

pulse also ends and the CHAR IN PROG signal (that has been enabling the Z Enable Gate) goes low. This completes the resetting of the Character Generator in the normal sequence.

Echoplex Suppress. When either the Graphic Input or the Graphic Plot Mode is initiated, the output of the Echoplex Suppress circuit becomes active. Its purpose is to prevent the Character Status circuit from responding to ENABLE signals generated by the $\overline{\text{ALPHA STB}}$ signal. In the Graphic Input Mode, data is sent from the Terminal to the computer. This data is placed on the data lines of the minibus. Therefore, the Echoplex Suppress circuit prevents the Character Generator from responding to that data.

The two signals that will reset the Echoplex Suppress circuit are, $\overline{\text{LOCAL}}$ and $\overline{\text{TBUSY}}$. The $\overline{\text{LOCAL}}$ signal becomes active when the LOCAL/LINE switch on the Keyboard is placed in the LOCAL position. This low active signal causes $\overline{\text{ECHO INH}}$ (Echo Inhibit) to go inactive (high), thus allowing the Character Generator to print the Alphanumeric characters when in the Local Mode. $\overline{\text{TBUSY}}$ allows the Character Generator to switch back to Alpha Mode from Graphic Plot Mode. To accomplish this $\overline{\text{TBUSY}}$ must go active.

TC-2
BLOCK DIAGRAM DESCRIPTION

Introduction

Refer to the TC-2 Detailed Block Diagram. As in the case of TC-1, TC-2 can be divided into blocks which perform specific functions. When possible, each block will be described as a separate entity. However, in some cases, it is difficult to obtain an over-view of circuit operation by discussing each block as an entity. In such cases, groups of blocks will be described in a sequence of operations (such as those needed to generate the crosshair cursor).

Below is a list of blocks that contain the greater part of TC-2 circuitry. A short description of each is given.

X Latch, Y Latch—data latches used when operating in the Graphic Plot Mode; provide storage for three 5-bit bytes of the 20-bit coordinate address.

X and Y Registers—each Register contains three 4-bit up-down counters, whose 10 bits of output data can be set by serial or parallel inputs.

Top-of-Page Detect Circuit—in the Alpha Mode, this circuit keeps the display beam in the viewable area of the Y Axis.

Margin Shifter—sets Margin 0 (left side of Display) or Margin 1 (center of Display).

Terminal Busy—places the Terminal in a "busy" condition, inhibiting the placing of data on the minibus by the keyboard, computer, or any other device that might be connected to the minibus.

X and Y Digital to Analog (D/A) Circuits—convert the digital outputs of the X and Y Registers into their equivalent analog voltage.

X and Y Filters—in the Alpha Mode, these circuits will not affect the output of the X and Y D/A's. In the Graphic Plot Mode they are enabled to provide a linear rate of change for the X and Y signals.

Data Multiplexer—depending upon the output of the Multiplexer Control circuit, the Data Multiplexer will place one of eight data bytes onto the minibus.

Strobe Logic—provides a signal that enables the Data Multiplexer to place the data bytes onto the minibus; also provides strobe signals to enable the computer and/or the Terminal to accept and process data.

Bits 6 and 7 Logic—places the complement of keyboard bits 6 and 7 onto their respective minibus data lines; also codes $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ with each 5-bit byte of data from the Data Multiplexer when operating in the Graphic Input Mode.

Multiplexer Control—controls the output of the Data Multiplexer; also inputs various signals to the Strobe Logic circuit to aid in the generation of the strobe signals, and aid in the digitization of the voltage from the X and Y Position Pots.

Crosshair Generator Circuitry—generates the crosshair cursor by sending a sequence of pulses that increment the X and Y Registers. With each register increment, a Z axis pulse is generated to draw the point. Rapidly counting through the Registers provides a crosshair type cursor, bright enough to be visible, yet dim enough so as not to store.

Z Control Circuit—(Circuit Cards 670-1729-05 and above)—Controls vector intensity when vectors less than approximately one-half inch long are being drawn.

Block Description

X and Y Data Latches. The X and Y Data Latches are used in the Graphic Plot Mode to provide storage for three of the 5-bit coordinate address bytes. In this mode of operation, data is sent from the computer to draw graphics, charts, figures, etc. on the Display screen. It takes twenty bits of data to establish a new coordinate address. However, only seven bits of data can be received from the computer at any one time; therefore, each coordinate address is divided into 4 seven-bit bytes. Two of the bits contain code data, and are used to develop load signals ($\overline{\text{HIY}}$, $\overline{\text{LOY}}$, $\overline{\text{HIX}}$, and $\overline{\text{LOXE}}$). Each load signal then loads its respective 5 bits of coordinate data into the appropriate latches. The High Order Y bits are first sent from the computer. The $\overline{\text{HIY}}$ signal decoded from the two most significant code bits loads the remaining five data bits into the five Most Significant Bit (MSB) portion of the Y Data Latch. In like manner the Low Order Y and High Order X bits are loaded into their respective latches. When the fourth byte (Low Order X needed to complete the coordinate address) is received from the computer, $\overline{\text{LOXE}}$ parallel loads all 20 bits into the X and Y Registers. Notice that the Low Order X bits are presented directly to the low order X inputs of the X Register. No storage is needed because they are the last bits received.

X Register (Counter). The X Register is a ten-bit, up-down counter. It is loaded either serially by the $\overline{\text{LEFT}}$ and $\overline{\text{RIGHT}}$ signals or it is loaded in parallel by the ten

parallel inputs that contain the X coordinate address in graphic plot operation. In Alpha and Graphic Input Mode, the Register is loaded serially. Each low-going $\overline{\text{LEFT}}$ or $\overline{\text{RIGHT}}$ signal will decrement or increment the output one count. The 10 outputs provide a count from 0 to 1023. Each count represents one Tekpoint, which simply means that the display beam can be positioned to any one of 1024 separate locations in the X Axis.

Either the CR (Carriage Return), $\overline{\text{HOME}}$ or $\overline{\text{PAGE}}$ signal will reset the X Register to zero. $\overline{\text{HOME}}$ goes active when terminal power is initialized or when the RESET key is pressed. $\overline{\text{PAGE}}$ goes active when the Page key is pressed or Control characters ESC plus FF are received by the Terminal.

Y Register (Counter) and Top-of-Page Detect. Like the X Register, the Y Register is loaded either in series (by $\overline{\text{UP}}$ or $\overline{\text{DOWN}}$) or in parallel when receiving 10 bits of data from the Y Data Latch. This register is also capable of outputting a count of 0 to 1023. In the X Register, all 1024 of the separate tek-points are viewable. In the Y Axis only 780 of the 1024 tek-points are viewable. When a $\overline{\text{PAGE}}$ or $\overline{\text{HOME}}$ signal zeros the Y Register (the outputs of the Y Register are connected to inverters), the alpha cursor does not position to the bottom of the screen; instead, because of the inverters, it positions off the top of the screen in the Y Axis. Therefore, circuitry is needed to bring the alpha cursor in view, to the Home position (upper left). This is accomplished by the Top-of-Page Detect circuit.

When the Y Register is zeroed by $\overline{\text{PAGE}}$ or $\overline{\text{HOME}}$, the outputs from the inverters go high, positioning the display beam off-screen at a count of 1023. The two most significant bits from the inverters are sensed by the Top-of-Page Detect Circuit. When both go high, the Top-of-Page Detect circuit places the 614 kHz square wave on the $\overline{\text{DOWN}}$ line, and immediately the display beam begins moving in the down direction. When the count from the Y Register has incremented 256 counts, the 2nd MSB goes low, inhibiting the Top-of-Page Detector circuit and removing the 614 kHz signal from the $\overline{\text{DOWN}}$ line. Thus, the count is stopped at 767 (1023 minus 256 = 767). Notice, that the $\overline{\text{DOWN}}$ signal going active increments the Y Register. This is true because of the complementary fashion in which the Register is designed. Even though the $\overline{\text{DOWN}}$ pulses increment the Register, the actual output is decrementing because of the inverters on the output lines.

The MARG signal output is actually an eleventh bit of the Y Register, and constitutes a count of 1024. It goes high when the Y Register counts past the bottom line of the page (1023). This signal inputs to the Terminal Busy, Multiplexer, Margin Shifter and Found circuit (Part of Crosshair Generator circuits). Its purpose can be found in the descriptions of each of those blocks.

Terminal Busy. When activated, this circuit holds the Terminal in a "busy" condition. $\overline{\text{TBUSY}}$ goes active low when the $\overline{\text{COUNT IN PROG}}$ signal from the Top-of-Page Detect circuit goes low. This action prevents the reception of data when the Register is counting down to the Home position. This circuit also contains a strappable option that works in conjunction with the MARG signal from the Y Counter. In the event the User wishes to view a full page of alphanumeric data, the hardware strap on TC-2 can be installed to make $\overline{\text{TBUSY}}$ go active when spacing past the last line of type. To clear the condition the User must send the $\overline{\text{PAGE}}$ signal by pressing the PAGE key on the keyboard, or $\overline{\text{HOME}}$ by pressing the Reset key, or by sending control characters ESC and FF.

Margin Shifter. For the Margin Shifter circuit to function, the junction strap in the Terminal Busy circuit must be installed in the position that does not give an active $\overline{\text{TBUSY}}$ signal when MARG goes high. Margin 1 is set in the following manner. When in the Alpha Mode, both $\overline{\text{GIN}}$ and $\overline{\text{GRAF}}$ will be inactive. This allows an inactive $\overline{\text{GRAPHICS}}$ signal to be input to the Margin Shifter circuit. When MARG goes high (when spacing past the bottom line of type of the display screen), and a carriage return has zeroed the X Register, MARG and $\overline{\text{GRAPHICS}}$ combine to put a high on the Most Significant Bit (512) input to the X Digital to Analog circuit. This enables the X D/A circuit to set a constant output voltage level that corresponds to the center of the Display Screen. Repeated Carriage Returns will not set the 512 bit low as long as the MARG and $\overline{\text{GRAPHICS}}$ signals are high. $\overline{\text{PAGE}}$ or $\overline{\text{HOME}}$ will inhibit Margin 1 by resetting the X and Y Registers to zero (the Y Register must be zeroed to set MARG inactive).

X and Y Digital to Analog (D/A) Circuits. These circuits convert the digital outputs of the Registers into their respective analog values. Both consist of a diode switching network. Depending upon the logic state of the Registers, the D/A circuits will cause a voltage change to occur on the outputs. Notice also, that the X and Y Matrix signals (X MAT, Y MAT) from the Character Generator in TC-1 are summed in their respective D/A circuit.

X and Y Filters. The outputs of the X & Y D/A Analog circuits are input to their respective filter. When operating in the Alpha or GIN Mode, $\overline{\text{NOLT}}$ (No Linear Interpolation) will be low. This allows the X and Y analog voltages to pass directly through the circuit to minibus pins M and P.

The Filter circuits are put in use when drawing vectors in the Graphic Plot Mode. When the Graphic Plot Mode is set, $\overline{\text{NOLT}}$ goes high, activating linear filters within the X and Y Filter circuits.

When $\overline{\text{LOXE}}$ simultaneously loads the 20 bits of data into the X and Y Registers, it causes an almost instantaneous change in voltage to occur at the outputs of the X and Y Digital to Analog circuits. This sudden change in voltage cannot be sent directly to the Display Amplifiers because the rate of change is non-linear. In other words, the vector drawn might be very fast at the start and very slow at the end; thus, hardly storing at the beginning and storing very bright at the end, or maybe even over-shooting the defined end point. The filter network overcomes these problems. It provides a linear rate of change in the X and Y output voltages to feed the Deflection Amplifier circuitry.

Data Multiplexer. The purpose of the Data Multiplexer is to place five bits (one byte) of data on to the minibus. There are 8 different bytes of data that the Multiplexer will place on the minibus. These include the Keyboard bits (b1-b5), Terminal Status Bits, High Order X bits, Low Order X bits, High Order Y bits, Low Order Y bits, Carriage Return bits, and End of Text (EOT) bits. The type of byte being placed on the minibus depends on the state of the 0–7 State Counter circuit.

When data is being sent from the Keyboard the 0–7 State Counter will be in its "0" state. This causes the 5 least significant bits of the keyboard character to pass directly through the Multiplexer and onto the minibus lines. Thus, for this type of operation it acts as a Keyboard to minibus interface. Keyboard data cannot be placed onto the minibus lines until the DATA ENABLE signal from the Strobe Logic circuit goes high. This happens when KSTROBE goes high. (More will be explained about KSTROBE in the description of the Data Logic circuit.) The other types of data bytes are used in the Graphic Input Mode and will be covered in the descriptions of circuits to follow.

$\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ are placed on the minibus through a special gating network labeled BITS 6 and 7 Gating. When data is being sent from the Keyboard, the Step Counter will be in State 0. This state allows the gating circuit to place the complements of keyboard Bits 6 and 7 on the minibus when the DATA ENABLE signal goes high as previously explained. BIT 8 is not used in the 4010 logic. During the transmission of the graphic input data, the State Counter outputs sets $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ low.

Strobe Logic. This circuit mainly controls the various strobe signals associated with Terminal and/or computer operation. $\overline{\text{CSTROBE}}$ is generated when data is destined for computer use. $\overline{\text{TSTROBE}}$ is generated when data is destined for Terminal use. $\overline{\text{ECHO}}$, which is usually held to ground by a hardwire strap on the Interface card, will enable $\overline{\text{TSTROBE}}$ when sending data to the computer in Line operation, thus providing a local copy on the screen of data sent to the computer. $\overline{\text{LOCAL}}$ originates from the Local Line switch on the Keyboard. It directs input sources to assert $\overline{\text{TSTROBE}}$ to provide a screen display of Keyboard data when operating in Local.

KSTROBE goes active high when data is entered from the keyboard. It is used to generate the $\overline{\text{TSTROBE}}$ and $\overline{\text{CSTROBE}}$ signals that route data to its destination. For example, if operating in Local, $\overline{\text{LOCAL}}$ will be active low, directing the Strobe Logic circuit to generate $\overline{\text{TSTROBE}}$; thus the Keyboard data is routed only for Terminal use and not for use by the computer. If operation is Line, KSTROBE directs the Strobe Logic circuit to generate $\overline{\text{CSTROBE}}$; thus routing the Data bits to the computer (if $\overline{\text{ECHO}}$ is low, $\overline{\text{TSTROBE}}$ is also generated). When entering data from the Keyboard, each time $\overline{\text{TSTROBE}}$ or $\overline{\text{CSTROBE}}$ is generated, the DATA ENABLE signal must go high to allow the Data Multiplexer to place the five Keyboard bits onto the minibus.

$\overline{\text{KLOCK}}$ is normally held high on the minibus. Should the User ever have need to inhibit the Keyboard, pulling $\overline{\text{KLOCK}}$ low will prevent KSTROBE from affecting the Strobe Logic circuit, thus providing a Keyboard lock.

$\overline{\text{CPUNT}}$ is asserted by the Interface Card to prepare the Terminal for data reception from the computer. $\overline{\text{DRBUSY}}$ is asserted by the Hard Copy Unit, inhibiting the Strobe Logic circuitry until it has completed making a copy of the display.

BITS 6 and 7 Logic. When sending data from the Keyboard, this circuit places the complements of Keyboard bits (b6 and b7) onto their respective minibus lines. When operating in the Graphic Input Mode, coding signals from the State Decoder set $\overline{\text{BIT 6}}$ and $\overline{\text{BIT 7}}$ low.

Z Control. This circuit is used only in Graph Mode while drawing vectors. It is then enabled by a high $\overline{\text{NOLI}}$ signal. When $\overline{\text{LOXE}}$ initiates a vector, the circuit becomes armed and a 10 μs delay is initiated. If the vector being drawn is less than approximately one-half inch, the three clock pulses (307 kHz, 153 kHz, and 77 kHz) combine to hold $\overline{\text{CGZSUP}}$ low for 11.4 μs out of every 13 μs. The 1.6 μs pulses generated while $\overline{\text{CGZSUP}}$ is high cause dots to be written on the screen. These dots are close enough together to appear as a continuous line. If the vector being drawn is more than approximately one-half inch long, the X D/A or Y D/A signal is large enough to reset the circuit before the 10 μs delay elapses, preventing $\overline{\text{CGZSUP}}$ from going low. The beam is then permitted to be left on during vector drawing.

Crosshair Generator. The Crosshair Generator contains the circuitry needed to generate the crosshair cursor. Its purpose is to reflect the digital equivalent of the X & Y Position Pots at the output of the X & Y Registers. The crosshair cursor is generated by alternately incrementing the X and Y Registers. This alternately sweeps the display beam left-to-right and top-to-bottom on the CRT.

The Crosshair Generator is activated when $\overline{\text{CURSE}}$ goes active. $\overline{\text{CURSE}}$ inputs to the Found circuit and sets $\overline{\text{FOUND}}$ high and FOUND low. $\overline{\text{FOUND}}$ enables the Clock circuit which begins sending CLOCK pulses to the Axis Switching and Switch Control circuits. The FOUND signal going low also causes the Strobe Logic circuit to output a low active $\overline{\text{GIN}}$ signal which inputs to U67B; thus, inhibiting the Top-of-Page Detect and Margin Shifter circuits. $\overline{\text{CURSE}}$ also presets the Axis Switching circuit to output a low going $\overline{\text{DOWN}}$ pulse each time the Q output of the Clock circuit pulses high. Each time the $\overline{\text{DOWN}}$ line pulses low, the Y register increments, causing the display beam to move down one tekpoint. With each beam movement, the 38 kHz STEP pulse causes an active $\overline{\text{Z}}$ signal from U309A (U44C on TC-2 boards with numbers 670-1729-04 and lower) to write (but not store) the point.

As the Y Register increments, moving the display beam downward, the output from the Y D/A circuit changes accordingly. It is monitored by the Y Comparator circuit in

the Crosshair Generator. When the Y Register has incremented to the point where the voltage from the Y D/A equals, or slightly passes, the voltage from the Y Position Pot, the Y Comparator sends a low $\overline{\text{Y COIN}}$ signal to the Memory Gates. While the $\overline{\text{DOWN}}$ line is pulsing, the DOWN signal from the Axis Switching circuit to the Memory Gates is high. When $\overline{\text{Y COIN}}$ goes low, the Memory Gates output a low $\overline{\text{SET}}$ signal to the Switch Control circuit. FOR TC-2 BOARDS WITH NUMBERS 670-1729-04 AND LOWER, THE FOLLOWING OCCURS: The next $\overline{\text{Q}}$ CLOCK pulse clocks the low $\overline{\text{SET}}$ signal into the Switch Control circuit, causing the $\overline{\text{STEP INH}}$ signal to U67D to go low. This inhibits further STEP pulses that were activating $\overline{\text{DOWN}}$ and $\overline{\text{Z}}$ signals. On the next positive going Q CLOCK pulse, the $\overline{\text{SWITCH}}$ signal goes high. When the positive portion of the Q CLOCK pulse ends, the $\overline{\text{SWITCH}}$ signal goes low, putting a low on the DOWN line and a high on the RIGHT line. FOR TC-2 BOARDS WITH NUMBERS 670-1729-05 AND UP, THE FOLLOWING OCCURS: When $\overline{\text{Y COIN}}$ goes low, the Memory Gates output a low $\overline{\text{SET}}$ signal to the Switch Control Circuit. The next $\overline{\text{STEP}}$ pulse clocks the low set signal into the Switch Control circuit, which enables the $\overline{\text{INHIBIT}}$ signal. $\overline{\text{INHIBIT}}$ prevents further $\overline{\text{STEP}}$ signals from activating $\overline{\text{DOWN}}$ and $\overline{\text{Z}}$ signals. On the next positive-going STEP pulse, the $\overline{\text{SWITCH}}$ signal goes high. When the positive portion of the STEP signal ends, the $\overline{\text{SWITCH}}$ signal goes low, putting a low on the DOWN line and a high on the RIGHT line. THIS ENDS DIFFERENCES IN CIRCUIT OPERATION FOR THIS PARAGRAPH.

FOR TC-2 BOARD NUMBERS 670-1729-04 AND LOWER: The end of the high Q CLOCK pulse also causes the $\overline{\text{STEP INH}}$ signal to U67D to go high. Once again, U67D outputs STEP pulses to the Axis Switching circuit. This time the $\overline{\text{RIGHT}}$ line is being pulsed because of the high on the RIGHT line.

FOR TC-2 BOARD NUMBERS 670-1729-05 AND UP: The end of the high STEP pulse also causes the $\overline{\text{INHIBIT}}$ signal to U309A and Axis Switching circuit to go high. Once again U309A begins outputting active $\overline{\text{Z}}$ signals. Also, with $\overline{\text{INHIBIT}}$ high, the $\overline{\text{RIGHT}}$ line can be pulsed because of the high on the RIGHT line.

FOR TC-2 BOARD NUMBERS 670-1729-04 AND LOWER: With U67D enabled, the clock circuit sends out pulses through U67D to generate $\overline{\text{Z}}$ and $\overline{\text{RIGHT}}$ signals until the X Register reaches or slightly passes the value selected by the X Position Pot. When this happens, the output of the X Comparator goes low. With the RIGHT signal from the Axis Switching circuit high, the Memory Gates will output another low SET signal to the Switch Control circuit. This low permits the Crosshair Generator circuitry to switch from X to Y in a manner similar to that described for Y to X switching.

FOR TC-2 BOARD NUMBERS 670-1729-05 AND UP: With U309A enabled, STEP pulses the $\overline{\text{Z}}$ line until the X Register reaches or slightly passes the value selected by the X Position Pot.

Foldover. Each time the X Register counts through zero, the display beam must reposition to the left side of the screen. The Register can reset much faster than the display beam can be positioned to the left. Therefore, the counting sequence is interrupted for a short period of time to allow the beam to position to the left and stabilize. When the X Register reaches a count of 1023 the Margin Shifter circuit outputs a low $\overline{\text{EOL}}$ (End of Line) signal. This signal is felt by the Fold Pause circuit in the Crosshair Generator. $\overline{\text{EOL}}$ triggers a one-shot multi within the Fold Pause circuit, causing $\overline{\text{FPAUSE}}$ to go low for .5 ms. $\overline{\text{FPAUSE}}$ then inhibits the output of the Clock circuit, preventing further $\overline{\text{RIGHT}}$ pulses. After .5 ms $\overline{\text{FPAUSE}}$ ends and the X Register continues to increment.

No pause is needed in the foldover of the Y Register. This is because when the Y Register sets back to zero, the display beam is positioned off-screen. By the time the Y Register increments enough to bring the display beam in view, it has had adequate time to stabilize.

The above operation of the Crosshair Generator continues until the mode is changed or until the 0 to 7 State Counter is incremented to respond to a Keyboard signal (Header Character) or an $\overline{\text{INQUIRE}}$ signal.

Multiplexer Control and Digitization. The Crosshair Generator reflects the digital equivalent of the X and Y Position Pots at the outputs of the X and Y Registers. The process of obtaining the digital equivalent of the position Pot voltages and sending this to the Computer in digital form is known as "digitization". Digitization occurs in a set sequence that is controlled by the Multiplexer Control circuit.

NOTE

The MARG signal must be inactive, otherwise digitization will not occur. This prevents a "page full condition" (terminal busy) when switching back to the Alpha mode.

To begin with, assume that the crosshair cursor is running as explained in the preceding description. The 0 to 7 State output is at State 0. When it is decided to send the point at which the crosshairs intersect, the user will strike a Keyboard key. This causes the Keyboard bits to be placed on the minibus by the Multiplexer and sent to the computer (see Fig. 6-7). When the computer has finished receiving the Keyboard data, $\overline{\text{CBUSY}}$ goes high, advancing the State Counter to State 1. When the Counter advances to State 1, the State Decoder circuit outputs a low on the STATE 0 line which inputs to the State Counter. With STATE 0 low, the State Counter will be able to advance one count each time $\overline{\text{CBUSY}}$ goes inactive (high).

The STATE 0 signal in conjunction with the 614 kHz timing signal will next cause a $\overline{\text{PREP}}$ signal to be sent to the Strobe Logic circuit. This causes the $\overline{\text{GO DIGITIZE}}$ signal to go low. The next time the Crosshair Generator reaches

DATA MULTIPLEXER TRUTH TABLE

The X is irrelevent when used to indicate an output.

STATE 4 C Pin 11	STATE 2 B Pin 10	STATE 1 A Pin 9	Keyboard Bit D0 Pin 4	Terminal Status Bit D1 Pin 3	HIX Bit D2 Pin 2	LOX Bit D3 Pin 1	HIY Bit D4 Pin 15	LOY Bit D5 Pin 14	CR Bit D6 Pin 13	EOT Bit D7 Pin 12	OUTPUT Y Pin 5
0	0	0	0	X	X	X	X	X	X	X	0
0	0	0	1	X	X	X	X	X	X	X	1
0	0	1	X	0	X	X	X	X	X	X	0
0	0	1	X	1	X	X	X	X	X	X	1
0	1	0	X	X	0	X	X	X	X	X	0
0	1	0	X	X	1	X	X	X	X	X	1
0	1	1	X	X	X	0	X	X	X	X	0
0	1	1	X	X	X	1	X	X	X	X	1
1	0	0	X	X	X	X	0	X	X	X	0
1	0	0	X	X	X	X	1	X	X	X	1
1	0	1	X	X	X	X	X	0	X	X	0
1	0	1	X	X	X	X	X	1	X	X	1
1	1	0	X	X	X	X	X	X	0	X	0
1	1	0	X	X	X	X	X	X	1	X	1
1	1	1	X	X	X	X	X	X	X	0	0
1	1	1	X	X	X	X	X	X	X	1	

Fig. 6-7. Data Multiplexer Truth Table.

coincidence, a $\overline{\text{PTFOUND}}$ signal is sent to the Found circuit. This causes $\overline{\text{FOUND}}$ to go low, inhibiting the output of the Clock and stopping the count at the Coincidence Point. The outputs of the X and Y Registers then reflect the digital equivalent of the voltage selected by the Position Pots. The low going $\overline{\text{PT FOUND}}$ signal also causes STATE 2 ADVANCE to go low, advancing the State Counter to State 2.

With the PREP signal and the FOUND signals now high, $\overline{\text{CSTROBE}}$ and DATA ENABLE from the Strobe Logic circuit will activate. When DATA ENABLE goes high, the Multiplexer will sample the 5 most significant bits (High Order X) of the X Register and send them along with BIT 6 and $\overline{\text{BIT 7}}$ coded by the Bit 6 & 7 Logic circuit) to the computer. When the bits are received by the computer, $\overline{\text{CBUSY}}$ once again goes high, advancing the State Counter to State 3. In turn, the Low Order X, High Order Y and Low Order Y bits are sent to the computer. The State Counter has now advanced to State 5. At this point it can either return to State 0 or send the Carriage Return (CR) bits and/or the End of Text (EOT) bits. This action is dependent upon the placing of the Option Straps.

The computer can request the coordinates of the crosshair cursor independent of the user. First it must send ESC plus SUB causing $\overline{\text{CURSE}}$ to go low to initiate the Crosshair Generator. The computer can then send ESC plus ENQ, causing $\overline{\text{INQUIRE}}$ to go low and the circuitry responds just as though $\overline{\text{CBUSY}}$ had been received after a Keyboard character was sent as previously described.

NOTE

A 20 millisecond delay must occur between ESC and SUB and the sending of ESC plus ENQ. This delay provides sufficient time for both X and Y coincidence to occur.

The computer can also request another form of Graphic Input data independent of the User. This is known as Terminal Status information. For example, when the computer sends ESC plus ENQ, $\overline{\text{INQUIRE}}$ goes low. This causes the State Counter to advance to State 1, sending the Terminal Status bits MARG, $\overline{\text{GRAF}}$, $\overline{\text{NOLI}}$, $\overline{\text{HCU}}$ and $\overline{\text{AUXSENSE}}$ to the computer. The circuitry then responds just as though $\overline{\text{CBUSY}}$ had just been received after a Keyboard character was sent as previously described.

DISPLAY UNIT

Display Unit Block Diagram Description

See the block diagram of the Display Unit (exclusive of Keyboard and hard copy consideration) in the pullout pages. The writing portion of the Display Unit consists of a High Voltage and Z Axis circuit, a Deflection Amplifier circuit, X and Y Deflection Coils, and the writing components of the CRT—namely the Cathode, Control Grid, and Focus Anode. The storage section consists of the Storage circuitry and the storage components of the CRT—the Flood Gun Cathode (FGC), the Flood Gun Anode (FGA), the Collimation Electrode (CE), and the Storage Backplate (STB). The writing portion of the display unit controls beam positioning and writing, while the storage portion controls and maintains the intensity of stored information.

Positioning information is received in the form of X and Y analog signals into the Deflection Amplifiers. These generate a positioning current in the X deflection coil and Y deflection coil, and also cause a DYNAMIC FOCUS signal to be sent to the High Voltage and Z Axis circuit. This DYNAMIC FOCUS signal is minimum for center screen positions, and maximum for edge positions. (Dynamic Focus is necessary because focusing is partially dependent on beam travel distance, and the beam must travel further in reaching the edges of the CRT than it does in reaching the center of the CRT.) The $\overline{\text{FUZZ}}$ signal is high during alphanumeric operation to provide uniform focusing throughout the CRT area. During Graphics operation, $\overline{\text{FUZZ}}$ goes low and permits optimum focusing of graphic vectors. The $\overline{\text{Z}}$ signals into the High Voltage and Z Axis circuit control the Grid Bias. The $\overline{\text{HCU INT}}$ signal modifies the CRT intensity to accommodate hard copy operation. Additional information regarding hard copy writing is available elsewhere in this section.

The storage circuitry responds to two input signals and provides the cathode-ray tube with four operating voltages. Assuming that $\overline{\text{PAGE}}$ and VIEW are both high, the Flood Gun Cathode continuously emits electrons which are accelerated by the Flood Gun Anode. These strike the Storage Backplate where they continuously reinforce the stored information. If no inputs are received by the Terminal for approximately 90 seconds, the signal goes low, causing the Flood Gun Anode voltage to drop to a level below that of the cathode. This reduces the flow of electrons from the Flood Gun Cathode and drops the CRT Intensity below viewing level.

The $\overline{\text{PAGE}}$ signal causes the CRT and Storage circuits to go through an Erase cycle. The four storage signals then cycle through a change in voltages which causes the CRT to become totally written and then to completely erase. A description of this cycle of operation follows.

HIGH-VOLTAGE AND Z AXIS CIRCUITS

Block Diagram Description. Refer to the block diagram of the high-voltage circuits. These circuits control the filament supply, the cathode supply, the control grid supply, and the focus supply for the writing gun of the CRT. A high voltage multivibrator drives a transformer to produce the various voltages required by the circuits. The multivibrator receives drive from one of the secondary windings and also receives biasing voltage for its control amplifier from a secondary winding. In addition, a high voltage feedback signal is applied to the multivibrator to keep the high voltage at a given value. CR71 and CR72 help to provide a −3850 cathode voltage supply, and filament voltage is obtained from a secondary winding of T50. The control grid circuit and filament circuit are both referenced to the −3850 power supply.

A tap from a secondary winding (which powers the high-voltage supply) sends additional voltage to the control-grid supply to enable it to provide a control-grid voltage which is more negative than the cathode voltage. The actual difference between the two is a function of the Intensity Control circuit and the Z Axis Signal Amplifier. If the $\overline{\text{HCU INT}}$ and $\overline{\text{Z}}$ signals are high, this difference is approximately 100 volts. When $\overline{\text{HCU INT}}$ is low, this difference increases to approximately 115 volts. When $\overline{\text{HCU INT}}$ is high and $\overline{\text{Z}}$ is low, this difference becomes approximately 50 volts, permitting stored writing to occur.

Another secondary winding of T50 provides the Focus Supply circuit with enough drive to develop negative high voltage for the focus anode. Focus Adjust permits optimum overall focusing. A dynamic focus amplifier works in conjunction with the high voltage focus supply. The DYNAMIC FOCUS signal compensates for defocusing due to the writing beam deflection from CRT center to CRT edge. There are two dynamic focus adjustments. Alpha Focus provides for uniform character focusing throughout the display area in Alphanumeric Mode. The Vector Focus adjustment permits optimum vector focusing, and is only effective during Vector Modes when $\overline{\text{FUZZ}}$ is low.

High-Voltage Oscillator. Refer to the High-Voltage schematic diagram. Oscillator Q101 provides current to the primary winding of T50. When current in this winding is increasing, a secondary winding provides positive voltage to the base of Q101. When Q101 collector current reaches Beta times its base drive, Q101 unsaturates and the primary winding voltage decreases. When the voltage at the base of Q101 becomes sufficiently low, Q101 stops conduction, causing a further decrease in the primary voltage. This causes a negative voltage to be applied to the base of Q101, driving this transistor further into cut-off. When C47

discharges sufficiently, the voltage at the collector of Q103 rises and the cycle repeats itself. The Q101 drive current is obtained by charging capacitor C47. However, part of the C47 charging current is also obtained from Q103. Therefore, changes in Q103 collector current affect the drive to Q101. Q103 current is controlled by a feedback from the high-voltage circuit, adjustable by R82.

High-Voltage Supply. Power for this supply is provided by the 8-13 winding. Voltage from this secondary is doubled by C70, CR71, CR72, and C72. The filtered −3850 volts is then applied to the cathode of the CRT. The unfiltered high voltage is connected through R67 and R68 to the two sides of the filament supply, elevating it to the proximity of the voltage on the cathode.

Control-Grid Supply. The −3850 cathode voltage is felt on C93, via CR94, R93, and R92. Assuming that pin 14 of the transformer is at zero volts, C93 charges to 3850 volts. With $\overline{\text{HCU INT}}$ high, the voltage at the wiper of R130 is at approximately +100 V. During one-half cycle of operation, pin 14 of T50 goes positive, with R130 limiting the bias signal to about +100 V at the R86-CR130 junction. This causes C93 to charge an additional 100 volts, ending up with approximately 3950 volts across it. Assume that $\overline{\text{HCU INT}}$ and $\overline{\text{Z}}$ are both high. The voltage at the top of DS154 is then at approximately +5 volts. When pin 14 of T50 swings negative, CR90 conducts and clamps the bias signal from going below +4.5 V. However, the 95 volt decrease on one side of C93 causes the other side to decrease by an equal amount. As the high voltage side of C93 goes negative to −3945, CR94 becomes back-biased. Since the low-voltage side of C91 is at approximately +5 volts, C91 now charges toward −3945 volts. With C91 charged to −3945 V, the CRT grid is placed 95 volts below the cathode voltage, blanking the writing beam.

Intensity Control Circuit. When the Hard Copy Unit is not in use, $\overline{\text{HCU INT}}$ is high, permitting Q35 to conduct. This places about 0.2 volt on the negative input of U119. U119 (a high-gain operational amplifier) and Q115 form a non-inverting voltage input feedback amplifier. Its +173 V output is set by the R104 current multiplied by the value of R105 resistance. With Q35 conducting, the Hard Copy Intensity adjustment ($\overline{\text{HCU INT}}$) has no effect.

The +173 volts from Q115 is applied to the Q37 circuit where approximately 100 volts is selected at the wiper of R130. (This is variable between approximately 55 and 145 volts due to CRT bias requirements.) This voltage is then used as mentioned in the Control Grid Supply description.

When a hard copy is commanded, the $\overline{\text{HCU INT}}$ line goes low, turning Q35 off. This causes the voltage at the negative input of U119 to go positive, depending on the setting of R103. The change in voltage at the negative input to U119 is matched at the U119 positive input, thus increasing current through R104. This current increase produces a higher voltage across R105, increasing the +173 V to a new level (not to exceed 213 V). This causes the voltage at the wiper of R130 to increase by the same amount. This increase permits C93 in the Control Grid Supply circuit to charge to a higher value when the bias signal at the CR130-R86 junction goes positive. With the voltage at the top of DS154 still +5 volts, C91 is permitted to increase its charge accordingly, increasing the voltage difference between the Control Grid and the cathode of the CRT. This increase in bias is necessary for hard copy operation.

When $\overline{\text{Z}}$ goes low to command the beam to write, the Beam writing voltage at the top of DS154 pulses to one of several different levels. These levels are dependent on the mode of operation. When operating in alpha, the voltage level is approximately 45 volts; when making a Hard Copy the level will be up to 8 volts above the alpha level. When operating in graph (vector plot) the voltage level is approximately 75 volts. The beam writing voltage at the top of DS154 is controlled by the base of voltage of Q99, and it is this voltage that is dependent upon the mode of operation.

When in Alpha Mode, $\overline{\text{FUZZ}}$ is low, switching Q98 on by way of CR117. With Q98 on, CR115 conducts, placing about 14.5 volts at the R117-R115 junction. This provides a biasing network for the base of Q99 that consists of R115-R114-R116. This combination provides Q99 with a bias voltage of about 45 volts.

When making a hard copy the $\overline{\text{HCU INT}}$ signal, by way of CR119, has similar effect upon voltage at the base of Q99. However, the voltage at the top of R114 increases because of the $\overline{\text{HCU INT}}$ signal through CR96. This causes the voltage at the base of Q99 to be as much as 8 volts above that caused by $\overline{\text{FUZZ}}$. The actual difference is determined by the setting of the Hard Copy Intensity control R103.

When in Graphic Plot mode ($\overline{\text{FUZZ}}$ is high) and a hard copy is not being made ($\overline{\text{HCU INT}}$ is high), Q98 is not conducting, thus preventing CR115 from conducting. This effectively deletes R115 as a biasing component for Q99. This allows the base potential for Q99 to be pulled up to about 75 volts.

Z Signal Amplifier Circuit. When $\overline{\text{Z}}$ is high, Q53 is turned on via bias network R140, R143, R144, R145 and R146. Q53's collector pulls down to about +6 V. Diode CR144 keeps Q53 from saturating for turn-off speed considerations. This is used as a reference voltage for the Control Grid Supply circuit as previously explained.

When $\overline{Z}$ goes low to command the beam to write, Q53 cuts off and its collector voltage rises toward +175 volts. However, the biasing voltage for the base of Q99 holds the emitter voltage of Q57 to either 45-53 or 75 volts, depending upon the mode of operation. When the collector of Q53 rises to the voltage value on the emitter of Q57, CR121 goes into conduction and holds the collector of Q53 at that value. This voltage now replaces the +5 volts that had been present at the top of DS154.

The change in voltage at the top of DS154 has an effect on the CRT Control Grid Bias. When the bias signal at the CR130-R86 junction drops to approximately 50 volts, CR90 goes into conduction and holds it at that value rather than permitting it to go to +5 V as before. The voltage swing at the CR90-C93 junction is therefore limited to +50 volts. In addition, since the low-voltage side follows suit, this decreases the voltage difference between grid and cathode to approximately 50 volts, permitting information to be written on the CRT. L149 increases the switching action during writing time, by helping to overcome the capacitance inherent in the Control Grid circuit.

Focus Circuit. The Focus circuit is designed to provide optimum focusing in all modes of operation. The circuit consists of a floating Focus High-Voltage Power Supply, Alpha and Vector Focusing adjust circuits, a Constant Current circuit, an Operational Amplifier, and a grounded-base amplifier used as a logic switch.

Operation of the circuit during Alphanumeric Mode with the cursor in a corner of the CRT will be explained first. Under this circumstance approximately 8 volts of focus correction signal is received at the DYNAMIC FOCUS input. Since this 8 volts is applied to voltage divider R25 and R26, it causes approximately 0 volts at the negative input of amplifier U157. U157 drives Q153 until the Q153 collector voltage is sufficiently positive to drive the positive input of U157 to a point of balance with the negative input. With the positive input at 0 volts, no current flows through R21 or R20. In Alphanumeric Mode $\overline{FUZZ}$ is low, turning Q137 off. This enables Vector Focus Adjust R10. Constant current circuit Q135 causes 0.3 milliampere to enter the circuit through the Q135 collector. The 0.3 mA is the only current flowing through feedback resistor R22, setting the R22-R35 junction (via feedback operation) to 150 volts. Approximately 150 volts is therefore felt at the emitter of Q151, providing a reference voltage for one side of the floating Focus High Voltage Power Supply. The Focus High Voltage Power Supply generates approximately −3850 volts, just as the cathode circuit high voltage winding does. A portion of this voltage is picked off by the Focus Adjust potentiometer and applied to the Focus Grid of the CRT. Note that with Q137 cut off and 0 volts on both sides of R20, neither the Vector Focus or the Alpha Focus has any control; focusing is totally dependent upon the position of R64 for CRT corner focus.

When the beam is moved to the center of the CRT while in Alphanumeric Mode, the Dynamic Focus voltage returns to approximately 0. The R25, R26 voltage divider applies approximately −5 volts to the negative input of U157. This causes U157 to drive Q153 until its collector is sufficiently low to permit the positive input of U157 to reach the value present on the negative input—approximately −5 volts. With the Alpha Focus potentiometer near midrange, R20 and R21 now demand approximately 0.08 mA of current. With 0.3 mA available from Q135, this leaves approximately 0.22 mA available to flow through R22, indicating that the collector of Q153 must be at approximately +105 volts. The focus reference voltage at the emitter of Q151 is therefore approximately +105 volts. Since current now is flowing through R20, the Alpha Focus control is effective and can be made to set the Q151 voltage to any value between approximately 85 and 115 volts, thereby controlling the focusing of the display near center of the CRT.

When Graphics Mode is selected, $\overline{FUZZ}$ goes high and turns Q139 off. This causes Q137 to act as an effective short circuit enabling the Vector Focus potentiometer. As with the Alpha Focus control, Vector Focus R10 only has effect on the display when the CRT beam is not located at any of the extreme corners of the CRT.

In summary, the circuit allows R64 (Focus Adjust) to adjust for good corner focus, R20 (Alpha Focus) to adjust for best alphanumeric focus when $\overline{FUZZ}$ is low, and R10 (Vector Focus) to adjust for best center screen focus when $\overline{FUZZ}$ is high.

Miscellaneous Components. A number of neon lamps appear in various parts of the high voltage circuit. These lamps are intended primarily as arc protection devices. At any time a radical change occurs in the voltage of any section of the high voltage circuit, these lamps fire and cause the remainder of the circuitry to stay electrically close together to avoid breakdown between the circuits.

DEFLECTION AMPLIFIER DESCRIPTION

General

The Deflection Amplifier circuit uses the X and Y analog voltages and amplifies them to provide the drive signals to the X and Y deflection coils. This circuit also generates a dynamic focus signal which is used in the high-voltage circuit.

Block Diagram Description

Refer to the Deflection Amp block diagram. The circuits making up the deflection amplifiers are the X Absolute Value Amplifier, the Y Absolute Value Amplifier, the X^2 and Y^2 circuits, the $X^2 + Y^2$ Amplifier, the X Geometry Multiplier, the Y Geometry Multiplier, the X Deflection Amplifier, and the Y Deflection Amplifier.

The X and Y signals are each applied to three circuits within the deflection amplifiers. The X signal goes to the X Absolute Value Amplifier to generate a positive output signal regardless of the polarity of the X Input signal. Then it is squared and applied to the $X^2 + Y^2$ Amplifier. Here it is combined with the positive signal from the Y^2 circuit to develop the Dynamic Focus signal which goes to the X Geometry Multiplier and the Y Geometry Multiplier, as well as going to the high voltage circuits. The X input signal is also applied to the X Geometry Multiplier circuit, where it combines with the Dynamic Focus signal to generate an X Geometry signal. The X signal, X Geometry signal and a Feedback signal from the X Deflection Amplifier combine at the summation point at the input to the X Deflection Amplifier. The output of the X Deflection Amplifier provides the drive for the X Deflection coil. The Y Deflection Amplifier circuit functions in a similar manner.

Detailed Description

Refer to the Deflection Amplifier schematic.

Because of the similarity between the X circuitry and the Y circuitry, only the X circuits will be explained here. The X absolute value amplifier consists of two operational amplifiers, each of which has one input referenced to ground. If a negative signal is applied, U87A develops a positive-going output which back-biases CR64 and forward-biases CR65, permitting the signal to be felt at the emitter and base of Q85. The negative signal is simultaneously applied to the positive input of U87B, causing its output to go negative. CR68 becomes back-biased, preventing the signal from affecting the output. CR67 becomes forward-biased, permitting feedback to pin 6 to offset the input signal. If the X input goes positive, U87B develops a positive output, forward-biasing CR68 and transmitting the signal to Q85. The positive applied to U87A causes its output to go negative, back biasing CR65 and forward biasing CR64, holding pin 2 at ground potential.

X^2 amplifier Q85 is cut off under no-signal conditions. Positive voltages applied to R73 cause the transistor to conduct. However, the same positive voltage being applied to R73 is also applied to the R70-R71 voltage divider. This causes the current through one side of Q85 to be less than the current through the side which has its base grounded. The output signals taken from the collectors of Q85 are then approximately equal to the square of the input voltage. They combine with the signals from Q69 in the Y^2 Amplifier, with the resultant signal being applied to the push-pull inputs of U105. U105 develops an $X^2 + Y^2$ output which it applies to the emitter of Q65. Q65 has a portion of the X input signal applied to the base of one-half of the transistor, causing outputs at the collectors of Q65 which are approximately equal to $KX (X^2 + Y^2)$. These are applied to push-pull amplifier U65, developing an output signal which is used as geometry correction. A portion of this is picked off by R93 and applied through R94 to the summation point at pin 3 of U45. Here it combines with the X signal from R100, the positioning signal from R96, and the Feedback signal from R115. U45 responds by developing an in-phase output signal which drives pin 2 of U45 to a value equal to that at pin 3. Q47 amplifies and inverts the output of U45, applying it to complementary emitter-followers Q5 and Q7.

Under no-signal conditions, the R111-R112 junction is at zero volts, resulting in no current through the X Deflection coil. If U45 outputs a negative voltage, Q47 develops a positive at its collector which is felt through the emitters of Q5 and Q7. The R111-R112 junction goes positive, causing electron flow up through the coil. If the pin 6 output of U45 goes positive, Q47 delivers a negative through the base-emitter junctions of Q5 and Q7, causing electron flow down through the X Deflection coil. Q67 provides relatively constant current to Q47 to optimize its operation.

It should be noted that operational amplifier U45 is located within the encompassing operational amplifier which includes inverter Q47, emitter-followers Q5 and Q7, and the feedback network which includes R117. Although the summation point is the positive input of operational amplifier U45, inverter Q47 causes the summation point to be the negative input of the total X Deflection Amplifier.

STORAGE CIRCUITS

Block Diagram Description. Refer to the block diagram of the storage circuits. The circuit controls the storage and erasure of data on the face of the CRT. The storage circuit consists of the following sections: The Fade Positive Multivibrator, the Erase Multivibrator, Storage Backplate Amplifier, Collimation Electrode Control, Collimation Electrode Amplifier, and View Control.

With $\overline{\text{PAGE}}$ high and low the output voltages are at the levels shown in the waveform diagram (on the same page as the storage block diagram). When a VIEW signal is received, the anode voltage goes positive, permitting stored information to become bright enough for viewing on the CRT. Data can then be written.

When a $\overline{\text{PAGE}}$ signal arrives, it causes the CRT face to become flooded, causing storage to occur over the entire screen. Immediately following this, the voltage is lowered to a point where all stored data erases. The sequence which causes this starts with the low going $\overline{\text{PAGE}}$ signal arriving at the Fade Positive Multivibrator. This causes a 12 millisecond low pulse to go to the View Control circuit, causing the anode and cathode to decrease their voltage by approximately 100 volts as shown in the waveform diagram. Simultaneously, the Fade Positive Multivibrator applies a 12 millisecond high pulse to the Collimation Electrode Control circuit where it initiates a negative-going $\overline{\text{DR BUSY}}$ signal. $\overline{\text{DR BUSY}}$ is applied to the Fade Positive Multivibrator to disable it until the erase cycle is completed. The 12 ms high pulse also causes the Collimation Electrode Amplifier to generate a 12 millisecond positive-going pulse on the Collimation Electrode Line.

When the 12 millisecond pulses from the Fade Positive Multivibrator end, the anode and cathode voltages from the View Control Circuit return to their quiescent value. The negative transmission into the Erase Multivibrator causes a signal to return to the Fade Positive Multivibrator, reinforcing the $\overline{\text{DR BUSY}}$ signal which prevents $\overline{\text{PAGE}}$ signals from entering. In addition, this signal from the Erase Multivibrator goes to the Collimation Electrode Control to sustain the $\overline{\text{DR BUSY}}$ signal and to change the Collimation Electrode Voltage to a value below that which occurs at quiescence. At the same time, the Erase Multivibrator causes the Storage Backplate Amplifier to drive the Storage Backplate Voltage to zero, from where it rises exponentially toward its previous voltage.

The signal from the Erase Multivibrator ends after approximately 700 milliseconds, causing the Collimation Electrode Control to set the Collimation Electrode Voltage positive for 12 milliseconds. When this 12 millisecond period expires, all voltages return to their quiescent levels.

Refer to the waveform diagram. The positive-going Collimation Electrode Voltage and the negative-going voltage on the Floodgun Anode and Cathode together cause flooding of the CRT Faceplate, providing uniform storage over the entire area. After the 12 millisecond pulses elapse, the collimation electrode returns to a value lower than quiescence to prevent any storing to occur until the end of the cycle. At the same time that the voltage pulses end, the Storage Backplate Voltage goes to zero to erase the face of the CRT. 700 milliseconds later the Storage Backplate Voltage has returned to normal, the Collimation Electrode Voltage returns to normal, and the $\overline{\text{DR BUSY}}$ signal returns high, indicating that erasing has been completed.

Detailed Description. Refer to the schematic of the Storage circuit. The Erase Multivibrator and Storage Backplate Control Amplifier (which determine the backplate voltage) will be discussed first. Under quiescent conditions, −15 volts is applied through R212, R211, and CR211 to hold Q35 in conduction. This causes Q55 to be in conduction with approximately −15 volts on its collector. The voltage at the R211, R212 junction is approximately −2.4 volts, causing C210 to charge approximately 12.5 volts. The base of Q57 is held at approximately −1.2 volts by the Q35 base-to-emitter junction and by CR211. This holds the emitter of Q57 at −1.8 volts, which holds the emitter of Q58 at −1.2 volts. Referring to Q39, it can be seen that its emitter holds its base at approximately +0.6 volt, holding the base of Q19 at zero volts. 1.2 volts thus exists between the emitter of Q58 and the base of Q19. With the Op Level control at mid-position, about 1/3 of a milliampere flows between the emitter of Q58 and the base of Q19. Very little of this passes through the Q19 base-emitter junction, leaving the majority of it to flow through R223. Multiplying this 1/3 milliampere by the R223 value (499 kΩ) provides approximately +180 volts at the emitter of Q95. The Q19, Q39, Q93, and Q95 circuit serves as a driver amplifier to sustain this voltage. The +180 volts at the emitter of Q95 is felt at the Storage Backplate Anode of the CRT.

After $\overline{\text{PAGE}}$ has been applied to U93 and the 12 millisecond multivibrator pulse expires, the negative transition is felt through C247 into Q55, turning this transistor off. Its collector goes toward zero volts. Since C210 has a 12.5 volt charge on it, the right side of this capacitor goes positive and the capacitor attempts to discharge through R210 and R212. The C210-R212 junction rises to approximately 12 volts and turns Q35 off. With Q35 cut off, its collector goes towards −15 volts, holding Q55 cut off. The positive voltage at the CR211-R211 junction is felt through the base-emitter circuit of Q57 and the emitter-base circuit of Q58. The positive potential at the emitter of Q58 causes zero volts to appear at the R219, R220 junction. With zero volts at the base of Q19, no current is demanded through

R222, and therefore none flows through R223. This causes the operational amplifier to place a zero volt output on the Storage Backplate (STB) anode.

During the next 700 ms, C210 discharges exponentially, changing the voltage being applied to the base of Q57. The STB voltage changes toward 180 V. After approximately 700 milliseconds, C210 discharges to the point where the voltage at the cathode of CR211 drops to about −1 volt, causing it and Q35 to go back into conduction. When this happens, the Storage Backplate voltage has been returned to its quiescent level. With Q35 in conduction, Q55 goes back into conduction, permitting C210 to again charge to its quiescent value.

Note that while Q35 is conducting, Q75 is held in conduction and places a low at pin 13 of U33F. This holds an enabling high on pin 5 of U93. However, during the 700 ns erase pulse, Q35 is cut off, holding Q75 cut off. The high Q75 collector voltage causes U33F to place a low on pin 5 of U93, blocking $\overline{\text{PAGE}}$ pulses until erasing has been completed.

The Collimation Electrode circuit will be discussed next. Under quiescent conditions, both inputs to U13D are low, placing a low at Pin 8 of U13C. This same low is felt at Pin 5 of U13B and is applied to R267. The low of R267 causes a high out of U33D. The U13B output remains low, causing a second low to be applied to U13C. The U13C output is therefore high, holding Q33 cut off. With Q33 cut off, its collector circuit delivers about one third of a milliampere of current to the null point at the base of Q77 in the Collimation Electrode Amplifier.

Since both inputs to U13A are low, U13A causes a low out of U33C, causing Q115 to be turned on. This holds about −0.2 V on its collector, delivering about 0.3 mA to the null point at Q77. In addition, R268 current flows into this point and is equal to about 0.25 mA. The combined currents flowing through R283 cause the output of the operational amplifier to be at approximately 80 volts.

When $\overline{\text{PAGE}}$ is received and the Pin 6 output of U93 goes high, U13D, U33A and U33D cause $\overline{\text{DR BUSY}}$ to occur. This is routed back to disable U93 so that no additional $\overline{\text{PAGE}}$ signals can affect the circuit until the erase cycle ends. Highs appear at the Pin 8 input of U13C and Pin 2 input of U13A. This causes Q33 to turn on and Q115 to turn off. The emitter circuit of Q33 now delivers about 0.13 mA, while the Q115 circuit delivers approximately 1.25 mA to the base of Q77. Again, this current combines with that from R268 and flows through R270, causing the output of Q97 to reach approximately 200 volts, which is applied to the Collimation Electrode of the CRT. When the 12 millisecond pulse from U93 expires, the high is removed from Pin 2 of U13A, causing Q115 to go into conduction. Since Q75 (in the Erase Multivibrator circuit) delivers a high to Pin 11 of U13D, a high is maintained on Pin 8 of U13C, holding Q33 in conduction. With both transistors in conduction, Q33 delivers about 0.13 mA while Q115 delivers about .03 mA. These combine with the .25 mA from R268. The current through R270 causes the Collimation Electrode Voltage to drop to approximately 30 volts.

This situation continues until the 700 ms erase period ends and Q75 is again put in conduction. At this time, Pin 11 of U13D goes low, applying a low at Pin 8 of U13C and Pin 5 of U13B. The low from the collector of Q75 is also applied to U107, which delivers a 12 millisecond pulse to Pin 6 of U13B. With lows on Pin 5 and Pin 6, U13B places a high on U13C and U13A. This causes Q33 to go into conduction and Q115 to turn off. The Collimation Electrode Voltage now rises to approximately 200 volts where it remains until U107 ends its 12 millisecond pulse. Then a high is placed at Pin 6 of U13B, putting a low into U13A and U13C. The outputs of these two devices return high, causing Q33 to turn off and Q115 to conduct. This restores the Collimation Electrode to its quiescent operating value of approximately 80 volts.

Note that the U13D output was low throughout the time the high 12 milliseconds pulse was being emitted by Pin 6 of U93, and during the time that Q75 was cut off. This causes U33A to apply a high to R267, charging C267. The resulting low from U33D held $\overline{\text{DR BUSY}}$ low, indicating that the CRT was erasing. In addition, when the collector of U75 went low, it caused U107 to create a 12 millisecond pulse which extended the low $\overline{\text{DR BUSY}}$ signal by that amount.

Notice that the $\overline{\text{WAIT}}$ signal inputs to the positive input of U93 and also holds the pin 6 input of U13B low. $\overline{\text{WAIT}}$ originates from the Hard Copy Unit (from those Hard Copy Units equipped with the Multiplexer option) and is used here to prevent an erase function during the time $\overline{\text{WAIT}}$ is active. (See the description of the $\overline{\text{WAIT}}$ signal in the Detailed Circuit Description of the Hard Copy Circuits.)

The View Control circuit quiescently holds the Flood Gun Cathode at approximately zero volts and the anode at about 150 volts. A voltage divider in the base of Q99 includes diode CR289, which conducts to hold the cathode near zero volts. Zener diode VR292 conducts to raise the voltage at the base of Q99 to approximately +150 volts. This is felt through the base-to-emitter circuit of Q99, where it is applied to the anode of the flood guns. Since U93 (in the Fade Positive Multivibrator) has its Pin 1 high under quiescent conditions, U33B delivers a low to the base of Q117, holding that transistor cut off. Zener diode VR287 conducts and causes +100 volts to be placed on the

left plate of C288. With the anode of CR289 very near ground potential, C288 charges to approximately 100 volts.

When a $\overline{\text{PAGE}}$ signal is received, Pin 1 of U93 goes low, causing U33B to deliver a high to the base of Q117. This transistor conducts and places the left plate of C288 near ground potential. With the left plate going negative by 100 V, the right plate is driven negative by an equal amount, placing a −100 V signal on the cathode of the flood guns. Since VR292 is still conducting, the voltage on the base of Q99 drops to +50 V. The cathode of Q99 and the CRT flood gun anode are thus caused to change in step with the CRT cathode voltage. After the 12 ms pulse from U93 elapses, the voltages return to their previous levels, 0 and +150 volts.

Under viewing conditions, the VIEW signal is high, holding Q135 cut off, which holds Q137 cut off and permits the just described situation to exist. However, when the viewing period has elapsed and the VIEW signal goes low, Q135 goes into conduction, causing Q137 to conduct. This back-biases CR291 and places approximately −15 volts on the base of Q99. The Q99 cathode voltage and flood gun anode voltage drop to about −15.6 V turning the flood gun off and dropping the CRT intensity below viewing level.

HARD COPY CIRCUITS

Block Diagram Description. If the Terminal is equipped with Hard Copy option, the circuitry shown in the Hard Copy Block Diagram is incorporated. Its overall purpose is to provide the Hard Copy Unit with a command for initiating a hard copy and then supplying the Hard Copy Unit with writing information, coincident with data stored on the CRT.

Whenever the Hard Copy Unit is attached and energized, a $\overline{\text{HCU}}$ signal is presented to the Terminal to advise of its availability. Whenever a $\overline{\text{MAKE COPY}}$ signal is initiated at the Display Unit, or is initiated by an ESC ETB sequence from the computer, the $\overline{\text{MAKE COPY}}$ command is applied to the Hard Copy Unit where it causes several outputs. A $\overline{\text{READ}}$ signal and a $\overline{\text{WAIT}}$ signal are applied to the Terminal to indicate that a hard copy is being made. This causes the Terminal to generate a $\overline{\text{DR BUSY}}$ signal to disable Keyboard and computer inputs to the Terminal. The Terminal also generates an $\overline{\text{HCU INT}}$ signal to modify the cathode and control grid voltages of the Display Unit writing circuits. $\overline{\text{READ}}$ causes the Deflection circuits to select X and Y inputs from the Hard Copy Unit rather than from the Terminal circuits. In addition, the $\overline{\text{READ}}$ signal places enabling voltages on the Z circuit and the TARSIG circuits within the Deflection Amplifier and Storage board.

The Hard Copy Unit provides a positive-going slow ramp to the Y Deflection circuits in the Terminal to cause the Terminal to sweep vertically one time. As it sweeps, a succession of fast ramps is supplied to the X Deflection circuits. This causes repetitive horizontal sweeps during the vertical sweep. The ramp signals are supplied to the readout circuits in the Hard Copy Unit at the same time they are being provided to the Terminal, permitting both units to be evaluating the same point on the display.

During each fast ramp, the Hard Copy Unit supplies repetitive $\overline{\text{INTERROGATE}}$ signals to the Terminal. These cause $\overline{\text{Z}}$ signals to be sent from the Deflection Amp and Storage board to the High Voltage and Z axis board in the Display Unit. There they cause a change in the writing gun control grid voltage, turning the writing beam on. If writing exists on the storage backplate in the position indicated by the deflection coils, the resultant current in the storage backplate circuit causes a TARSIG signal to be generated on the Hard Copy TARSIG Amplifier board. This is sent to the Pedestal section where it is gated through by the $\overline{\text{READ}}$ signal. This results in $\overline{\text{TARSIG}}$ being sent to the Hard Copy Unit. The Hard Copy Unit then writes a point at the position commanded by the fast and slow ramps. When the slow ramp ends, Hard Copy operation is discontinued and all signal lines except $\overline{\text{HCU}}$ return to their inactive status. Control of the deflection circuit is returned to the X and Y signals from the Terminal.

Detailed Circuit Description. Refer to the Hard Copy Selector schematic. If the Terminal is not equipped for Hard Copy, the X and Y signals are routed through a strap to the X and Y Deflection Amplifiers and none of the Hard Copy Selector components are contained on the circuit board. When the Hard Copy circuitry is included, the X and Y straps are removed and the circuitry is as shown. The X and Y outputs are each the output of one of two amplifiers, as selected by the Q105-Q125 circuit.

With Hard Copy not selected, the $\overline{\text{READ}}$ signal is high, placing a high on the base of Q105. This causes Q125 to place lows at the CR9-CR10 and the CR29-CR30 junctions. CR9 and CR29 are forward biased, placing lows at the positive inputs of U3 and U43. Their outputs are driven sufficiently low to back-bias CR4 and CR24, disconnecting the amplifiers from the output circuit. At the same time, diodes CR10 and CR30 become back-biased, preventing Q125 from affecting either U23 or U63. This permits the X and Y signals to control the X and Y outputs to the deflection amplifier circuit. Each amplifier has a gain of one, since the full voltage outputs are felt at the negative inputs of the amplifiers.

When a Hard Copy is commanded, $\overline{\text{READ}}$ goes low, causing the emitter of Q125 to go high. This places highs at the negative input of U23 and U63, causing their outputs to go low. CR11 and CR31 become back-biased, preventing U23 and U63 from affecting the X and Y outputs. CR9 and CR29 are also reverse-biased, permitting the HCX ramp and HCY ramp to control the X and Y outputs to the Deflection Amplifiers. The output amplitudes can be controlled by adjusting R4 and R22, which determine the amount of voltage being presented to the amplifiers. J51 (located in the output circuit) permits the X and the Y Deflection Amplifiers to both be controlled by the Y signal. This permits simultaneous application of equal drive signals to both axis for calibration purposes.

The $\overline{\text{READ}}$ signal also controls U81D, U103, U101B, and U101C. When $\overline{\text{READ}}$ is high, the outputs of these circuits rest at their inactive state. When $\overline{\text{READ}}$ goes low, $\overline{\text{HC INT}}$ goes low, $\overline{\text{DR BUSY}}$ goes low, $\overline{\text{TARSIG}}$ is put under the control of the TARSIG input signal, while $\overline{\text{Z}}$ is placed under the control of $\overline{\text{INTERROGATE}}$. While $\overline{\text{READ}}$ is low, U83 causes a $\overline{\text{Z}}$ pulse (0.2 to 0.6 μs, variable) to occur in response to each $\overline{\text{INTERROGATE}}$ signal. When $\overline{\text{READ}}$ returns high, U103 places a 150 microsecond low on U81B, holding $\overline{\text{DR BUSY}}$ low for that additional period.

The $\overline{\text{WAIT}}$ signal is an input from the Hard Copy Unit (if the Hard Copy Unit is equiped with the Multiplexer option). When the Terminal issues a Make Copy request, the Hard Copy Unit responds back to the Terminal with the $\overline{\text{WAIT}}$ signal. $\overline{\text{WAIT}}$ is used to hold $\overline{\text{DR BUSY}}$ active until

the Hard Copy Unit has completed making the copy. When the copy is completed $\overline{\text{WAIT}}$ and $\overline{\text{READ}}$ go inactive. $\overline{\text{READ}}$ going inactive causes U103 to fire, thus sustaining $\overline{\text{DR BUSY}}$ as explained in the preceding paragraph.

Refer to the Hard Copy TARSIG Amplifier schematic diagram. If the Terminal is not equipped with Hard Copy circuitry, T2 is connected directly to J2. With Hard Copy circuitry installed, T2 connects to J115 and J2 connects to J110. Inserting the Hard Copy TARSIG Amplifier board in the connector's path permits the STB current to be monitored. Since this current reflects whether a written or non-written area is being scanned, it provides information for the hard copy writing. Filtering is provided to the remaining T2-J2 lines to minimize circuit noise.

The storage backplate signals are coupled through T20 and applied to differential amplifier U5 which has a gain of approximately 400. Its output is amplified by approximately 10 in U45 and applied to comparator U65. U65 provides a negative output pulse in response to STB signals of an amplitude determined by threshold potentiometer R35. R35 permits the voltage at the positive input of U65 to be set between 0 and +2.3 volts. The U65 output pulses are applied to one-shot multivibrator U61, which responds by generating 20.4 μs (approximate) positive going TARSIG pulses.

LOW-VOLTAGE POWER SUPPLY

Refer to the Low-Voltage Power Supply schematic. This power supply has regulated outputs of −15 volts, +5 volts, and +15 volts. It also has unregulated outputs of −20 volts, +20 volts, +175 volts, +328 volts, and +503 volts.

The unregulated supplies will be discussed first. All of these except for +175 volts obtain their power from conventional, full-wave bridge rectifier circuits. The +175 volt supply uses a full wave center-tapped transformer configuration. The sources for the 503 volts, 328 volts, +175 volts and +20 volts are connected in series aiding, with each supply being referenced to the next lower supply. For example, three windings are in series to provide power for the +503 volt circuit. Two windings are connected in series to provide the power for the 328 volt output, etc.

Three fuses provide protection for the power supply circuits. F21 fuses the +15 volt and +20 volt supplies. F41 fuses the +5 volt supply and F61 fuses the −20 volt and −15 volt supplies.

Regulated Supplies

VR25 develops the 6.2 volts which is used as reference for the +15 volt and +5 volt supplies. A portion of this is picked off by R27 and is applied as reference to the positive inputs of U69 and U77. The regulated +15 volt output is applied through a voltage divider to the negative input of U69 to provide regulating drive to that amplifier. Outputs from U69 are applied through VR35 to Q29 to control the drive current to series regulator Q510.

The regulated +5 volts is applied through R44 to the negative input of U77. U77 compares this against the voltage at the positive input to generate a regulating output voltage, which is applied to Q75 to control the drive current to series regulator Q515. Q99 and Q97 provide the +5 volt circuits with over-voltage protection. Under normal conditions the +5 volts applied to the emitter of Q99 is insufficient to cause the device to conduct. If the +5 volt line should go as high as 5.5 to 7 volts, 1.2 volts at approximately 50 mA is applied to the gate of Q97. This causes Q97 to conduct, immediately lowering the +5 volt line to approximately 1 volt. The associated surge of current causes F41 to open up, removing power from the circuit.

The −15 Volt regulator uses ground for a reference at the input of U71. The negative input receives its signal from a comparison between the +15 volt supply and the −15 volt supply applied through voltage divider R57 and R58. Any deviations on the −15 volt line cause drive to U71 which provides a signal to the error amplifier Q73. This controls the drive to Q520, regulating the −15 volt supply.

HEAVY DUTY POWER SUPPLY

Refer to the H.D. Power Supply schematic 670-4216-00 and the drawing showing the component locations for the supply. This Heavy Duty supply may be used in place of the supply labeled "Low-Voltage Power Supply" to supply additional current for extra interface requirements.

When the instrument is equipped with the H.D. Power Supply, the power requirements will increase from a maximum of 192 to 235 watts. The shipping weight will increase about 5 pounds.

Line Voltage Straps

Power is supplied to the instrument from P500 through the power switch, fuse, filter, and line voltage straps to the transformer primary. The diagram is drawn showing the 100 to 120-volt strap plugged into the MED position for 115-volt ±10% line voltage. For 200 to 240-volt operation, use the 200 to 240-volt strap plugged into the appropriate position as shown on the diagram instructions. See Fig. 6-8 for the proper strap configurations. Note that one 200 to 240-volt strap can be used with two configurations by changing one pin to the appropriate pin 8 or 9 position. The unused strap is stored nearby plugged onto two ground pins on the circuit board.

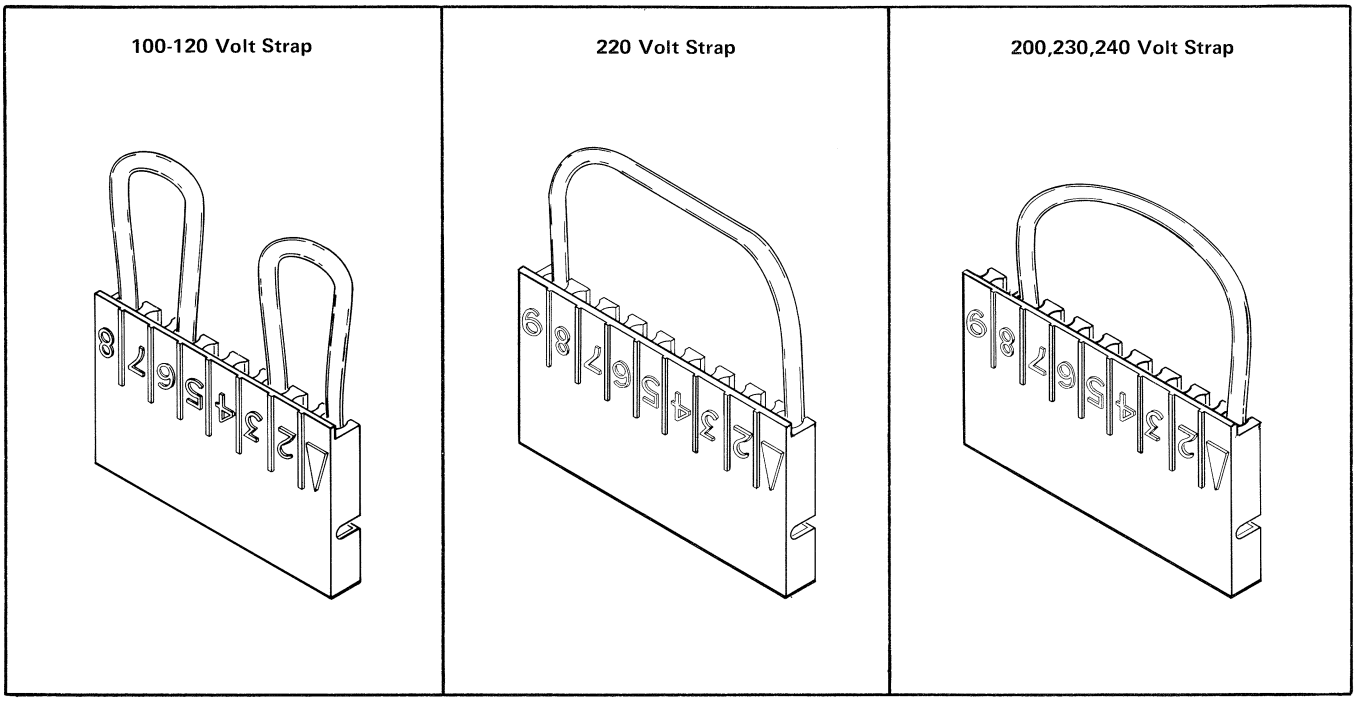


Fig. 6-8. Line Voltage Strap Configurations.

General Information

This supply has regulated outputs of −15, +5, and +15 volts. It also contains unregulated outputs of −20, +20, +175, and +328 volts. A regulated supply for the filaments in the CRT flood guns is referenced to the −20-volt unregulated supply.

Three fuses provide protection for the power supply circuits. F139 fuses the +15 and +20 volt supplies. F145 fuses the +5 volt supply and F135 fuses the −20 and −15 volt supplies.

Regulated Supplies

Voltage reference for the +15 and +5 volt regulated supplies is supplied by U175 and set by R27. The +15 volt regulated output supplies the voltage reference for the −15 volt supply. VR155, a 43-volt zener supplies reference for the CRT filament flood guns.

+15 Volt. U175 regulator drives Q178 to drive Q510 series pass transistor. Current limiting is provided by R177 and Q175.

U175 compares the +5-volt reference set by R27 and the +5 volts (from the +15-volt output through divider resistors R172 and R174). U175 output at pin 11 drives Q178 to drive Q510 to regulate the +15-volt output.

Supply current through R177 is limited to about 1.2 Amperes when the voltage across R177 turns on Q175 to turn off Q178.

+5 Volt. Regulation is accomplished by U170, Q65, Q270, and Q515. Current limiting and foldback functions add Q155, Q55, and Q61. For overvoltage protection, a crowbar circuit is used consisting of Q75 and Q80.

U170 compares the +5 volts reference set by R27 to the +5 volt supply voltage (+5-volt Sense, or if not used to the +5-volt supply output through R79). R72, C68, and CR69 are active on power up to prevent overshoot of the +5 volts. U170 output is amplified by Q65 and Q270 to drive the series pass transistor Q515.

Q155, VR158, and R157 form a constant current source which supplies current to the emitters of dual transistor Q55. Q55 forms a differential pair to sense the supply current through the current sense resistor R45. R156 sets the current (set at the factory for 10.6 A), at which current limiting begins. When an over-current condition occurs (above the condition set by R156), the output of Q55 causes Q61 to conduct and reduce the conduction of Q65 to lower the supply voltage. A further increase in supply current will result in a decrease in the supply voltage to a point of "foldback" (in the case of a short on the supply). The minimum output current of the supply for foldback is about 3 A, and is set by CR161 and CR165 biasing Q55.

The crowbar circuit is adjusted by R50 for 4.8 volts at the base of Q75. If the supply voltage exceeds 5.5 volts, Q75 turns on to turn on the crowbar SCR Q80 which pulls the +5 volts supply down to about 1 volt. Once the crowbar SCR is turned on, the power must be turned off and back on to release the SCR Q80.

−15 Volt. Variations in the −15-volt supply are monitored by the R272/274 divider resistors and cause U270 to regulate the −15-volt supply through Q275, Q278, and the series pass transistor Q520. Current limiting is provided by Q165 and current sense resistor R167. Q165 starts current limiting the supply at about 1.2 Amps and reduces the conduction of Q275, Q278, and Q520 to lower the output voltage.

Flood Gun Filaments. The regulated supply for the flood gun filaments is set by VR155 (a 43-volt Zener) and referenced to the −20 V unregulated supply. Q161 and Q265 regulate the filaments voltage with one end of the filaments connected to −20 V unregulated.

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF).
Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

Symbols used on the diagrams comply with USA Standard Y32.2-1970.

Logic symbology complies with ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The following special symbols are used on the diagrams:

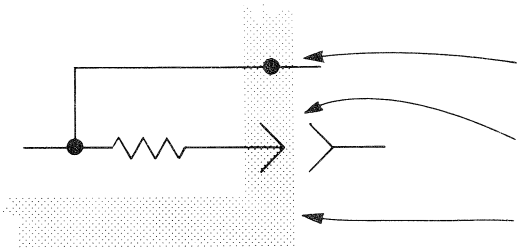
Screwdriver adjustment.

Clockwise control rotation in direction of arrow.

Refer to diagram number indicated in diamond.

Refer to waveform number indicated in hexagon.

Square-pin contacts for strap option contacts and off-board plug connectors.



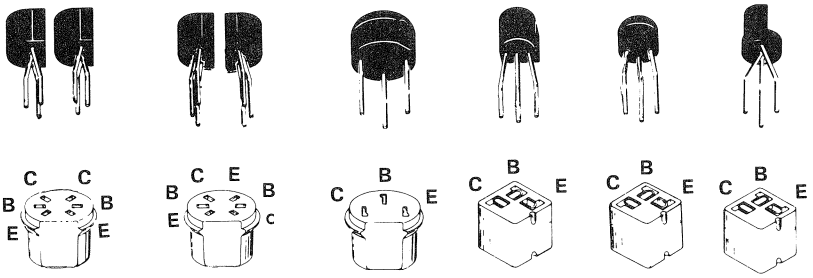
Connection soldered to circuit board.

Connection made to circuit board with interconnecting pin.

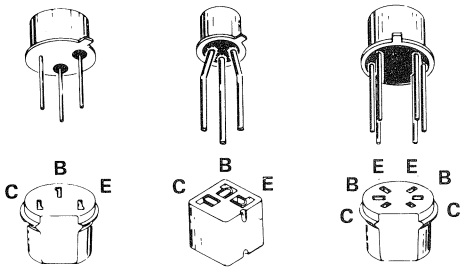
Tint encloses components located on circuit board.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

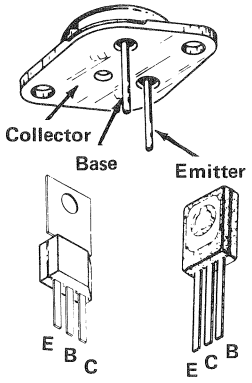
A	Assembly, separable or repairable (circuit board, etc.)
AT	Attenuator, fixed or variable
B	Motor
BT	Battery
C	Capacitor, fixed or variable
CR	Diode, signal or rectifier
DL	Delay line
DS	Indicating device (lamp)
F	Fuse
FL	Filter
H	Heat dissipating device (heat sink, heat radiator, etc.)
HR	Heater
J	Connector, stationary portion
K	Relay
L	Inductor, fixed or variable
LR	Inductor/resistor combination
M	Meter
Q	Transistor or silicon-controlled rectifier
P	Connector, movable portion
R	Resistor, fixed or variable
RT	Thermistor
S	Switch
T	Transformer
TP	Test point
U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
V	Electron tube
VR	Voltage regulator (zener diode, etc.)
Y	Crystal



Plastic-Cased Transistors

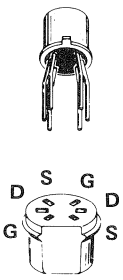


Metal Cased Transistors



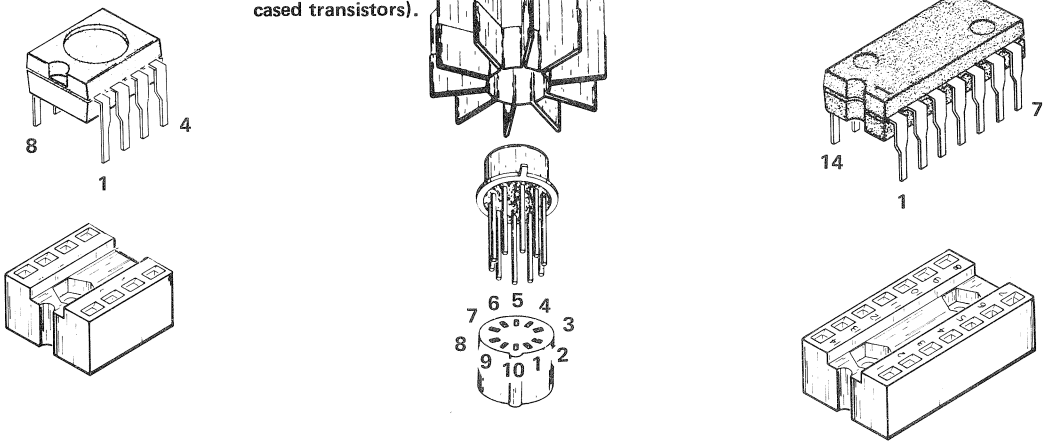
Power Transistors

FET



Dual FET

Heat dissipator (may be applied to some metal-cased transistors).



Integrated Circuits

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SEMICONDUCTOR INFORMATION

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