AFP-8 ASCII FRONT PANEL

USER'S MANUAL

TECHNICAL SPECIFICATION SUMMARY

and

DRAWING SET

Revision 1: 3 January 1977

dcq
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AFP-8 ASCII FRONT PANEL

USERS MANUAL

ABSTRACT

The AFP-8 is a console and front panel controller for remote and local PDP-8 minicomputers. This manual explains the functions and operation of the AFP-8. The information contained in this document is proprietary to Digital Communications Associates, Inc.

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Introduction

This document is designed to acquaint new users of the ASCII Front Panel (AFP-8) with the characteristics of the module. It also provides usage parameters for the unit.

Examples of the functions of the AFP-8 are provided to demonstrate proper operation.

The AFP-8 is a physical replacement for the KL8-E and KL8-JA Console Teletype Control. It is a single-thickness quad-board that is electrically and mechanically compatible with the PDP-8/e/f/m/a OMNIBUS. Insertion of the AFP-8 into any slot of the OMNIBUS is the sole installation criterion.

The AFP-8 can operate in parallel with or replace any KC8 Programmer's Panel.

Two different modes of operation are provided, i.e., Front Panel Mode and Teletype Mode. Explanation is given in the text for the operation of each of the modes.

The AFP-8 is independent of any software resident in the PDP-8. NO changes to DEC programs or user applications programs are required in order to substitute the AFP-8 for a KL8.

It is recommended that the first-time user of the AFP-8 read this entire document thoroughly before inserting the AFP-8 into the OMNIBUS. It is also recommended that the various examples be performed immediately after inserting the AFP-8 into the OMNIBUS, both as an initial test of the functions of the module, and as an exercise to become familiar with its operation.

A diagnostic procedure for the AFP-8 is provided on Page 21.

A brief technical specification is provided in the Technical Specification Summary.

The AFP-8 operates with the optional AFP Security Option (SO) for applications where the AFP-8 is connected to a direct dial network, and it is desirable to prevent access by unauthorized users. When used with either the optional, on-board modem, or the on-board, EIA compatible interface, a user must enter one of four, on-board selectable, 8-character ASCII passwords before he can gain access to the AFP-8, and thereby the PDP-8. Once the password has been verified by the SO, the SO becomes transparent.

The passwords are contained in field-replaceable PROM's. The SO also provides a local port which bypasses the password function. Any modem or terminal which can be connected to the AFP-8 can also be connected to the SO. All AFP-8 features are available when used with an SO. The SO is an OMNIBUS compatible quad module which connects to the AFP-8 by a 40 conductor cable.

Initial Installation

The AFP-8 should be examined visually for any damage resulting from shipment. If damage is observed, please contact DCA at once.

The AFP-8 is shipped from the factory with a cable to attach a terminal to the AFP-8. This cable should be plugged into the 40-pin connector (J01) at the upper left-hand corner of the AFP-8 module. Observe correct polarity of the connector as marked. If there is a dot on the connector, it should be visible when it is inserted. The other connector end (DB25S for EIA terminals, or a MATE-N-LOCK 8-pin for 20ma terminals) should be attached to the corresponding terminal connector.

The 40-pin connector provides the following configuration for initial operation of the AFP-8:

Baud-rate - 110
Echo - enabled
Front Panel Mode - enabled
Switch Register - enabled
External Clock - inhibited
IOT device codes - 603X, 604X

EIA terminals have DTR (Data Terminal Ready) and RTS (Request To Send) leads permanently asserted by the AFP-8. The 20ma Teletype terminal connection is pre-wired to utilize the READER-RUN control as does the KL8 control. See Section 2 for methods of programming the AFP-8 to other configurations.

If any other device on the OMNIBUS (such as an existing KL8) is configured with device codes conflicting with the AFP-8, the other device must be removed before installing the AFP-8. The AFP-8 IOT device codes can be re-programmed, as discussed in Section 2. For familiarization, however, let the AFP-8 physically replace the existing KL8.

Power Restart and Bootstrap options should also be removed or disabled for the examples in this manual to work as described. They may be re-installed or re-enabled during normal operations, because the AFP-8 is compatible with all OMNIBUS peripherals.

The AFP-8 may be inserted into any working slot of a standard OMNIBUS. If the installation replaces a KL8-E (M8360) or KL8-JA (M8655) connected directly to a Teletype, the cable already connected to the Teletype can simply be inserted into J01.

If the CPU has a KC8-EA Programmer's Panel, it must be set to the following configuration in order to avoid interference with AFP-8 functions:

Switch Register - all switches down
Rotary display switch - STATUS position
SW, Halt, and SS switches - "Up" position

The key position marked "Panel Lock" may be selected, since it does not inhibit the AFP-8.

No special configuration of existing equipment or modules is necessary if the AFP-8 is the sole source of Programmer's Panel functions. Use of the AFP-8 does the work of both the KC8 Programmer's Panel and the KL8, thereby saving one slot.

Initial Operation

The AFP-8 is intended for use by those who are familiar with the Programmer's Panel for the PDP-8/e/f/m/a. The AFP-8 functions closely follow the switches and displays of these panels, so users can quickly learn to substitute keyboard commands for the hardware controls and switches previously used.

It is strongly suggested that first-time AFP-8 users reproduce the examples in this document exactly as they appear. This speeds up learning, and also checks the AFP-8 to insure that it is functioning properly. After you have some experience with the AFP-8, the exercise on page 12 (to increment the AC) can be used as a quick check of the normal operation of the AFP-8. The Diagnostic (page 21) is provided to determine if the AFP-8 has a malfunction.

In order to assist the reader, Figure 1 (on page 4) is a comparison of the PDP-8 Programmer's Panel switches and readouts with the AFP-8's readout, control, and CPU function character substitutes.

Power Sequence

When the CPU power is turned on, the AFP-8 delays 0.9 seconds to allow all the power-up sequences to take place on the OMNIBUS, halts the CPU (unless the automatic restart is enabled), and then prints out a 5-digit message on the terminal:

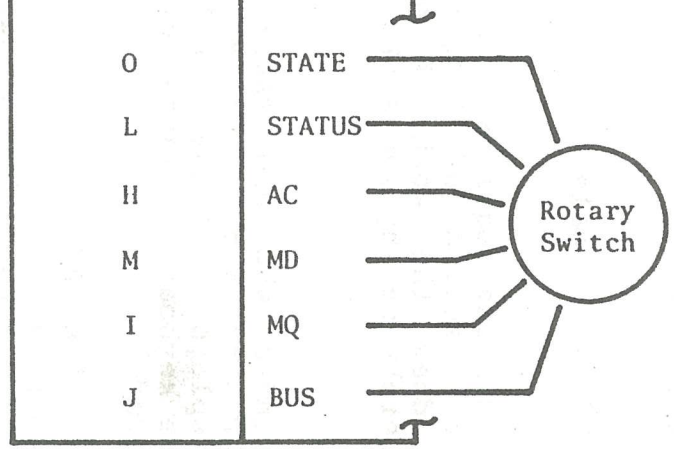
0XXXX

The first digit of this readout is explained later. It is zero in this example. The remaining four digits are the current content of the Memory Address lines on the OMNIBUS.

> WARNING: The first character which is typed after the power is turned on is often 'lost' by the AFP-8. It will still, however, be echoed to the console terminal. For this reason, it is good practice to check what was loaded into the SR, or to type a readout character as the first character when the CPU is powered up.

*AFP-8 Control Commands	HALT Set	SW Set	SS Set	HALT Clear	SW Clear	SS Clear
P				X	X	X
Q		X		X		X
R			X	X	X	
S		X	X	X		
T	X				X	X
U	X	X				X
V	X		X		X	
W	X	X	X			

AFP-8 Readout Substitutes	Front Panel Readouts
N	MA Read
O	STATE
L	STATUS
H	AC
M	MD
I	MQ
J	BUS



	SW	SWITCH REGISTER Ø 1 2	SWITCH REGISTER 3 4 5	SWITCH REGISTER 6 7 8	SWITCH REGISTER 9 10 11	ADDR LOAD	EXTD ADDR LOAD	START CLEAR	START CONT	EXAM	HALT	SING STEP	DEP
PDP-8 FRONT PANEL SWITCHES →													
AFP-8 FRONT PANEL COMMAND SUBSTITUTES →	Q*	First Digit	Second Digit	Third Digit	Fourth Digit	A	F	C	G	E	T*	R*	D

AFP-8 ASCII FRONT PANEL COMMAND SUBSTITUTES FOR PDP-8 FRONT PANEL COMMANDS

Front Panel Mode (FPM) vs. Teletype Mode

To operate both as a Programmer's Panel and as a Teletype control, the AFP-8 has two modes. It is important to recognize which mode the AFP-8 is in so you can give it correct commands. The AFP-8 is either in Front Panel Mode (FPM) or in Teletype mode. When in Teletype mode, it emulates the DEC KL8 under control of the program in operation. When in FPM, the red Light Emitting Diode mounted at the top center of the AFP-8 is lit.

The AFP-8 enters FPM whenever the CPU is halted for any reason. As the CPU halts, the MA register (current PC value) is typed out so the operator knows where the program stopped.

The AFP-8 also enters FPM if it detects a "framing error" from the keyboard. This framing error is a long-space (200 msec minimum) generated on most terminals by depressing the key marked "break", "attn", or "interrupt". "Break" is detected before the keyboard flag is set, so the PDP-8 CPU never sees the "break" command. "Break" causes the MA to be typed out, but the CPU is not halted.

The AFP-8 leaves FPM and enters Teletype Mode when a program starts, or when the CPU is already running in FPM and the "P" key is struck.

In summary, the MA is read out automatically if:

(1) "break" is detected (enters FPM, CPU continues to run);
(2) CPU halts (also enters FPM);
(3) Single Step instruction is executed (also causes "HALT" and enters FPM); or,
(4) power-up.

ECHO and ASCII Terminal Control Characteristics

When in FPM, the AFP-8 echoes input characters to the output terminal for visual verification of proper reception by the AFP-8 from the terminal. This is called the ECHO feature, and it can be suppressed by a wiring option (see Section 2 for further information). ECHO suppression may be desired for some local half-duplex (i.e., local copy) terminals. The AFP-8 does not work with half-duplex modems or communication circuits, as it does not provide a protocol to turn the line around.

All ASCII control characters (codes 0-37) are ignored, but echoed, by the AFP-8 while in FPM. These characters can be used to format the printed output. In particular, "CR", "LF", and "space" may be freely used to separate the function characters. These optional control characters improve the legibility of strings of AFP-8 functions.

The AFP-8 function keys may be either upper or lower case, since both perform the same functions.

Readout Functions ("H" through "O")

The AFP-8 does not have lamp displays as the DEC Programmer's Panel does. The substitution of 8 "readout" function keys (characters) provides information identical to the Programmer's Panel displays. These keys are the letters "H" through "O" on the terminal keyboard. Readout displays are provided by a 5-digit series, as explained below.

To illustrate their use, strike each character in the order shown to reproduce the same output on the terminal.

(Note: User keystrokes are underlined here and in all following examples).

Key	Description
H00000	Accumulator
I00000	Multiplier-Quotient Register
J00000	OMNIBUS Data Bus (clear unless some peripheral has a stuck bit)
K00000	The AFP-8 Internal Switch Register
L00000	CPU Status Display
M00000	Memory Data lines on the OMNIBUS (usually contents of memory when cycled)
N00000	Memory Address lines on the OMNIBUS
O02040	CPU State display (value not relevant here)

Note that the AFP-8 inserts a carriage return and line feed after each display, which returns the terminal printing to the left column. This happens for the readout functions only.

The digits in the readouts for "L" (Status) and "O" (State) are the same as the bits displayed by the Programmers Panel. These digits are explained in the DEC "Small Computer Handbook" corresponding to the model of PDP-8 in use. This handbook is supplied by DEC.

Interpretation of the First Digi t

All readout functions produce a 5-digit number. The first digit of this number is an octal encoding of 3 bits of important CPU internal state information. Bit 0 of this digit (i.e., with octal weight of 4) is the state of OMNIBUS RUN. Bit 1 of this digit (i.e., with octal weight of 2) is the OMNIBUS POWER-OK. Bit 2 of this digit (i.e., with octal weight of 1) is the OMNIBUS LINK signal.

Thus, the encoding of this digit is interpreted as follows:

First Digit	Run	Power	Link	Description
0	Halted	OK	0	Normal initial state
1	Halted	OK	1	Link set
2	Halted	Bad	0	Power supply failed
3	Halted	Bad	1	Power supply failed
4	Running	OK	0	Normal running, Link not set
5	Running	OK	1	Normal running, Link set
6	Running	Bad	0	Power supply and timing board failed
7	Running	Bad	1	Power supply, timing board, and CPU failed

Switch Register

The AFP-8 contains a 12-bit Switch Register (SR) that is logically identical to the Programmer's Panel 12-bit Switch Register, but is independent both for data entry and readout. AFP-8 input commands ("A", "D", and "F") use the SR to enter data into the CPU. The SR may also be used by programs (including MAINDEC's) as a program parameter.

If a Programmer's Panel is installed, its Switch Register is inclusively "OR"-ed with the AFP-8 SR. It must be clear (all switches down) for proper AFP-8 operations.

The AFP-8 SR can be changed/examined by the user only when the AFP-8 is in FPM. Numbers to be entered into the SR are typed as groups of 4 octal digits which are loaded into the 12-bit register sequentially from the left. Thus, the first digit is entered into bits 0-2 of the SR, the second digit into bits 3-5, the third digit into bits 6-8, and the fourth digit into bits 9-11.

In entering a digit, a mistake can be corrected by typing any non-numeric character, excluding control characters such as Carriage Return (this resets the internal AFP-8 pointer to the first digit's position), and then retyping all four digits of the correct octal number. Each current SR digit is replaced as you type in the new digit. Any remaining digit is undisturbed until a new value is entered. If more than 4 digits are typed, the internal pointer "wraps-around" to point to the first digit again.

To illustrate this, we will type numbers into the SR and examine the values in it with the "K" readout function (NOTE: The leading digit of the printout is 0 in these examples):

1234K01234 This shows that a 4-digit number can be checked immediately by the "K" function.

23K02334 The first two digits overwrote the leftmost two digits in the SR, but did not disturb the rightmost two digits.

56 7012K07012 Correcting typing errors was accomplished by typing a "space" and retyping the correct number.

0123456K04563 The first four digits (0123) were entered into the SR.

The next three digits overwrote the leftmost 3-digits of the SR with the new values (456), since the internal pointer wrapped around. The final digit was not disturbed, as only seven digits were typed (original four digits plus three digits overwritten).

43#1K01363 This is what happens when a line strike error wipes out one of the digits. The intention was to type "4361", but the "6" was changed (by the line hit) into a "#" which reset the pointer to the leftmost digit. The "1" therefore overwrote it. This illustrates the need to keep an eye on the echoed characters to correct for line errors.

4361K04361 The new number is entered correctly by retyping.

Control Functions ("A" through "G")

AFP-8 control functions operate only when the CPU is halted. They perform the operations of loading the Memory Address and Extended Address, depositing and examining memory, Clear, and Continue. To illustrate these functions, readout class functions will be used to display the CPU registers as we go. The following example shows how to load a program beginning at memory location 0200.

* The LOAD ADDR Function ("A" key):

0200AN00200 The SR is loaded with 0200, and LOAD ADDR is performed using the "A" key. The results are checked by using the "N" key to readout the MA register.

* The EXTD ADDR LOAD Function ("F" key):

0011FL00011 This illustrates the loading of the data and instruction fields registers of the Memory Extension Control, and their examination by use of the STATUS readout ("L") key.

If the CPU does not have a Memory Extension Control module (KM8-E or KM8-A), the "F" function is superfluous and the data and instruction field will always be read as zero. The "F" function loads only bits 6-11 of the STATUS Register, and does not affect bits 0-5.

Control Functions ("A" through "G")

* The DEPOSIT Function ("D" key):

Note: The program used in the following illustration consists of two instructions:

```
0200    7001    START,IAC       /Increment AC

0201    5200          JMP START     /Loop
```

0200AFN00200 Load Address 0200, clear fields, and check.

7001D5200D The contents of the SR are deposited into successive locations in memory. The MA register is incremented automatically after each deposition, duplicating the DEPOSIT key on the Programmer's Panel. (Notice that the "D" function does not provide a carriage return or a line feed.)

* The EXAMINE Function ("E" key):

0200AEM07001 To examine memory, reset the MA register to 0200
EM05200 by using the "A" function. The "E" function cycles memory, but display of the result is accomplished by the "M" function. Automatic incrementing provided by the "E" function permits successive locations to be displayed.

* The CLEAR and CONT Functions ("C" and "G" keys):

K00200 Check the SR to verify it is still at 0200.

T Make sure the machine is halted.

AFTCG00201 LOAD ADDR, EXTD ADDR LOAD, set the HALT switch (explained below), CLEAR ("C"), and CONT ("G"). The program runs for one instruction and halts immediately, which causes it to type out the MA.

G00200 The CONT Function ("G") key causes it to run for one more instruction and halt again, typing out the new MA contents.

H00001 The AC Readout Function ("H" key) is used to verify the operation of the program (i.e., increment the Accumulator.)

CH00000 The "C" function is used to clear the AC, which is verified by another use of the "H" function.

CPU Functions ("P" through "W")

The DEC KC8-EA Programmer's Panel has three switches used to control operation of the CPU. The SW is a control for the hardware bootstrap (if there is one installed, it should be disabled when performing the

following functions).

The HALT Switch stops the CPU after execution of the next instruction. When set, it performs the function of stopping the CPU after each instruction, which is useful in some debugging situations.

The SINGLE STEP (SS) Switch stops the CPU after every memory cycle, and is otherwise identical to the HALT Switch.

The AFP-8 implementation of these functions is accomplished by a micro-coding of the letters "P" through "W" as shown in the table on Page 14.

When any of these keys is struck, an internal 3-bit register of the AFP-8 is loaded with the value of the function as specified in the table. So, in the example of the single program just executed, the "T" function had the effect of clearing the SW and SS bits and setting the HALT switch in this internal register.

The CPU executes exactly one instruction each time the "G" function is executed, stops, and then prints-out the MA register. There is no way of interrogating the contents of the SS and HALT bits of this register except by their action on a program. The SW bit is displayed in the STATES readout display ("O" key).

The "P" ("Proceed" is a good mnemonic) key can be used to clear the SW, HLT and SS bits all at once. This is generally the key used before starting a program.

The AFP-8 leaves FPM when the CPU starts running, or is already running and the "P" key is struck.

To illustrate this, we use the two-instruction program already loaded in 0200-0201:

0200AFPCG Load Address, Fields, clear CPU Control Register, clear the CPU, and GO. This starts the program at 0200.

At this point, further keystrokes are ignored by the AFP-8, since they go to the portion of the circuit which is the Teletype controller, and this program is currently not addressing the Teletype controller.

Of course, the program IS counting up the Accumulator rapidly. To observe this, press the "break" key on the terminal.

40201 The CPU is running (the "4" in the first digit position tells us so) and the MA register is 0201. To see what is in the Accumulator, we use the "H" function.

H47632 The contents of the AC are changing rapidly, as we can easily verify with another "H" function.

H51437 Notice that the AC has overflowed into the Link, which is displayed as the low-order bit of the first digit. To demonstrate that we have control over the program, we use the CPU Halt function ("T" key).

T10201 We see that the Link is still set, and the MA is at 0201.

H15422 The Accumulator has incremented some more.

CH00000 When we clear the CPU, the link and the Accumulator are also cleared. Let us continue the program from here.

PG ....and the program is now running again. Tough question for the operator: why did we type the "P" before the "G"?

(The values in the right-most 4 digits are not duplicatable in the user's test example, but serve only to illustrate the principles).

Additional Examples

Let us now look at some other examples of the operation of the AFP-8 in FPM and in Teletype mode. The first sample program is as follows:

0000A Load address 0000

7604D Deposit an LAS (Switch Read) at address 0000

5000D Deposit a JMP to 0000 at 0001

Now that this simple program has been entered into memory, the input commands "C" and "G" are utilized. The following example loads address 0000, clears the AC and LINK, and starts the processor:

0000AFPCG

The sample program is now running. To monitor what is going on, we enter FPM and use the output commands. The entry into FPM is accomplished via the "BREAK" key.

Readout of the major registers can be performed as follows:

H40000 Machine running; AC loaded with 0's
I40000 Machine running; MQ has all 0's
J40000 Machine running; BUS 0:11 = 0's
K40000 Machine running; SR 0:11 loaded with 0's
L40000 Machine running; STATUS = 0's
M47604 Machine running; executing 7604 (LAS)

```
N40001     Machine running; looping at location 0001
O44640     Machine running; F,IR=6, MD DIR=1
```

Remember, in FPM with the CPU halted, the two-character command "EM" will perform an examination of the present location.

Let us stop the processor by using the "T" command and perform a few readouts.

```
T00001     Indicates machine halted at location 0001
EM05000    Examine shows JMP instruction at 0001
N00002     Shows "E" command performs PC PC+1
```

All FPM functions have been presented with simple examples. The following more sophisticated example uses most of the commands to show how they can be utilized manually, both to program and to monitor a program.

```
N01746          Indicates machine halted at location 1746
0000AN00000     Load Address 0000 and check address
7001D           Deposit IAC (increment AC) at location 0000
2020D           Deposit ISZ on location 0020 at 0001
5001D           Deposit a JMP to location 0001 at 0002
5000D           Deposit a JMP to location 0000 at 0003
0000AN00000     Load Address 0000 and check address
EM07001         Examine memory location 0000
EM02020         Examine memory location 0001
EM05001         Examine memory location 0002
EM05000         Examine memory location 0003
AN00000         Load Address 0000 and check address
PCG             Clear HALT, clear AC and LINK, and CONTINUE
```

This program increments the AC with approximately 16msec delay. At this point, assume we press the "BREAK" key and perform the following:

```
H40074     AC Read indicates machine running with AC = 0074
H45477     AC Read indicates machine running with AC = 5477
H50161     AC Read indicates machine running with LINK set
           and AC = 0161
T10001     HALT program.  Readout indicates machine halted
           with LINK set at location 0001.
```

The next example illustrates the operation of the AFP-8 both as a Front Panel and as a Teletype control. Assume the processor is not running. (Each command line is terminated with a carriage return and line feed by the user to make the example more readable).

The example program to be entered is essentially a Teletype ECHO test.

AFP-8 ASCII FRONT PANEL 1/3/77
Additional Examples

KEY	CODE	COMMENTS
0000A		Switch Register set to 0000; Load Address
F		Clear Memory Extension
6032D	KCC	Clear Keyboard Flag and AC; advance Reader
6031D	KSF	Skip on Keyboard Flag
5001D	JMP.-1	Jump to 0001 (loop 'til Flag)
6036D	KRB KCC	Read Keyboard Character; Clear Flag
6046D	TLS	Load Teleprinter sequence
6041D	TSF	Skip on Teleprinter Flag
5005D	JMP.-1	Jump to 0005
5001D	JMP 1	Jump to 0001
N00010		Check the MA contents to see that it's what was expected
0000A00000		Load Address 0000 and check address
EM06032		Examine MD. Note RUN is off (first octal character = 0)
EM06031		Examine memory
EM05001		to see
EM06036		if it's
EM06046		what was
EM06041		just now
EM05005		deposited...
EM05001		The program is OK, so now execute it
0000A		Load Address 0000 again
F		Clear Fields (not required, but good practice)
P		Clear the SW, HALT, and SS switches
C		CLEAR (i.e., INIT)
G		GO (i.e., same as CONT switch)
ECHO TEST		Just to prove the CTY is working while the AFP-8 is not in FPM
40001		Pressing the "BREAK" key enters FPM, and prints the MA. The CPU is running, and is hung in a loop at 0001
1234A		Put a number into the SR and attempt to load address while the CPU is running
N40002		The LOAD-ADDR didn't work! (HALT not set)
T00002		Set the HLT switch to stop the CPU. CPU not running, but we are still in the loop
P		Clear the HLT
G		...and continue. We now enter non-FPM
ANOTHER ECHO		...which can be demonstrated. Enter FPM using "BREAK"
40002		MA shows JMP.-1 is next
T00000		Stop the CPU again
I00000		MQ has not been touched
J00000		BUS is not asserted
K01234		SR contains our new number
L00000		STATUS is zero
M06031		MD shows KSF is being executed
N00002		MA shows the JMP.-1 is next
O04640		STATES shows F,IR=6, MD DIR=1

Summary of AFP-8 Functions ("A" through "W")

This completes the keyboard commands to the AFP-8 while in Front Panel Mode. A summary follows:

Control Functions	Operations
A	Load Address SR 0:11
B	Unused
C	Clear AC and Link (Initialize)
D	Deposit SR 0:11
E	Examine MA Location
F	Load Extended Address (Fields) SR 6:11
G	Continue (CPU start = Go)

Readout Functions	Operations
H	ACCumulator read
I	MQ Register read
J	DATA bus read
K	SR 0:11 read (AFP-8 internal)
L	STATUS display read
M	MD bus read
N	MA bus read
O	STATES display read

CPU Functions	Operations
P	HLT and SW and SS clear
Q	SW set, HLT and SS clear
R	SS set, HLT and SW clear
S	SW and SS set, HLT clear
T	HLT set, SS and SW clear
U	HLT and SW set, SS clear
V	HLT and SS set, SW clear
W	HLT and SW and SS set

Send "BREAK" to enter Front Panel Mode.

Strike "P" to enter Teletype Mode while CPU is running in Front Panel Mode.

Start program to enter Teletype Mode.

I/O Configuration

A 40-pin connector (J01) is mounted on the upper left corner of the AFP-8. J01 provides signal paths, voltages, and grounds. Selection of combinations of pins connects the AFP-8 either to EIA RS-232-C or 20ma TTY terminals, as well as the options described below. See Figure 2-2.

The following describes pins on J01 used for serial-in and serial-out and the configuration of all other pins to accomplish operation in either EIA or 20ma mode.

Teletype Connection - 20ma operation utilizes six pins. Eight pins are used if Reader Run is provided. (See Fig. 2-1 below.)

Figure 2-1
20ma OPERATION

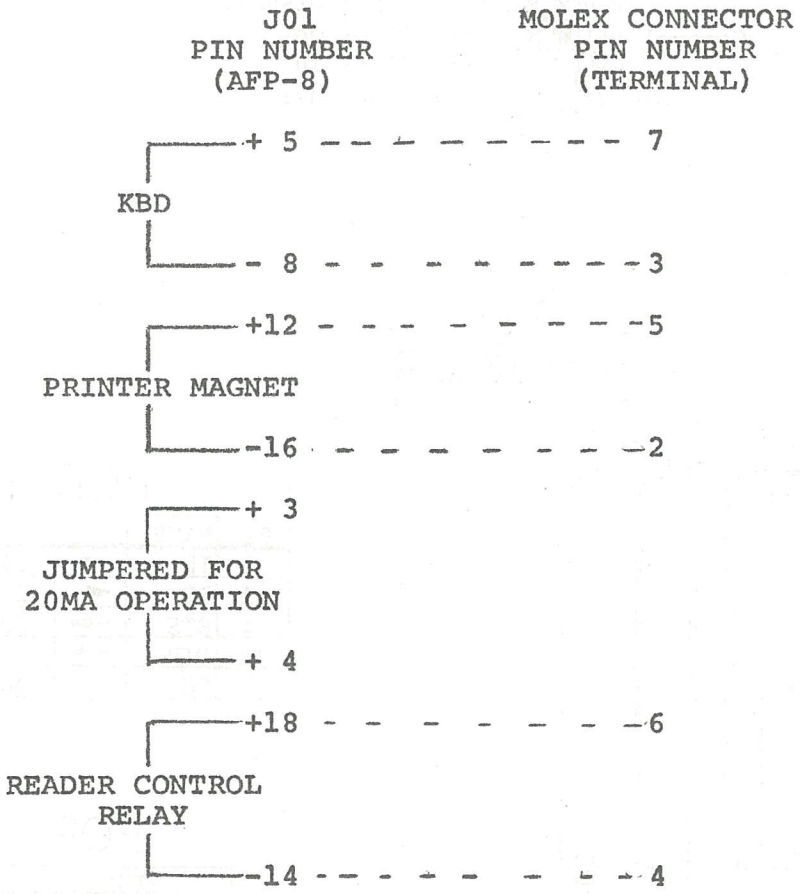
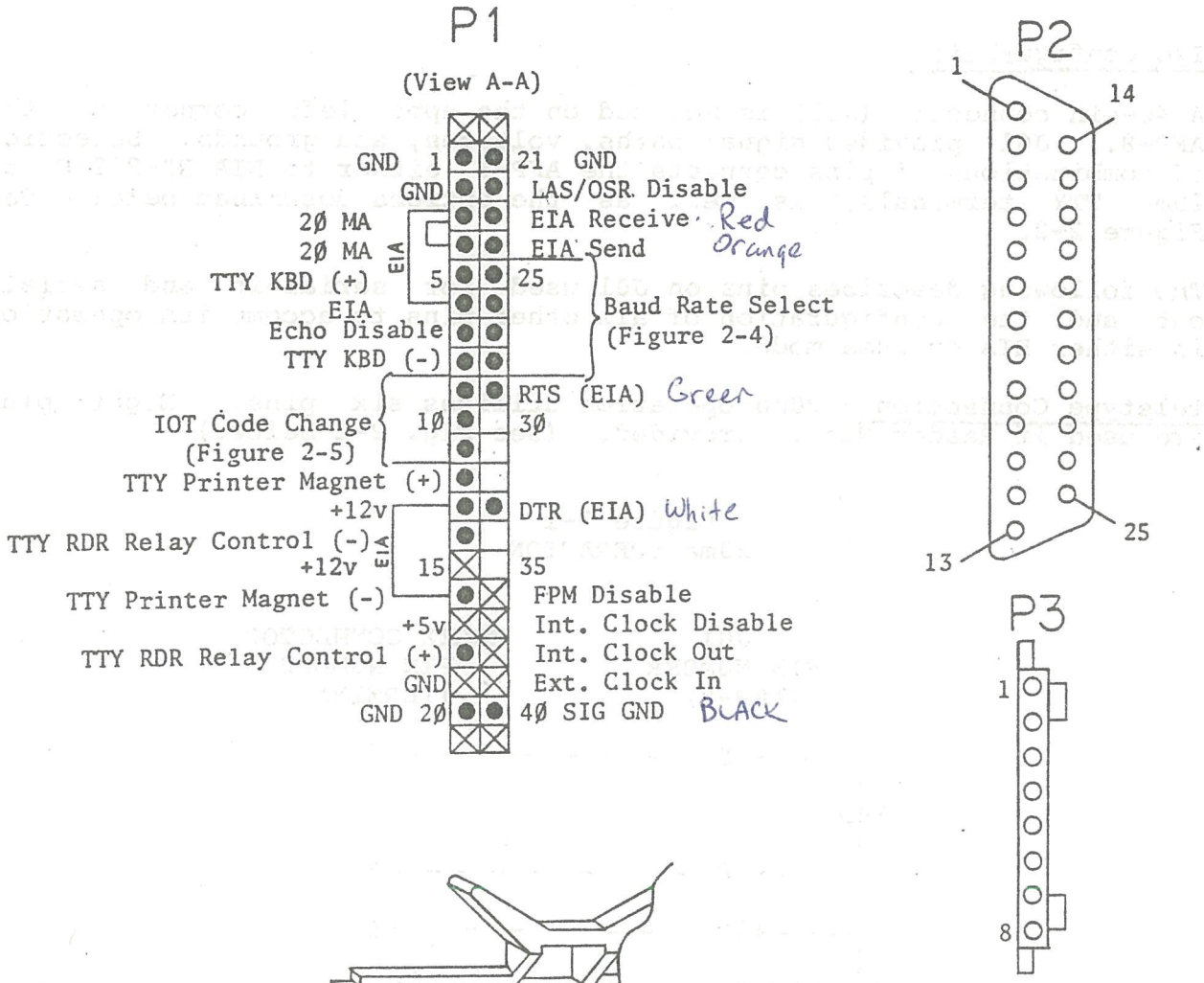
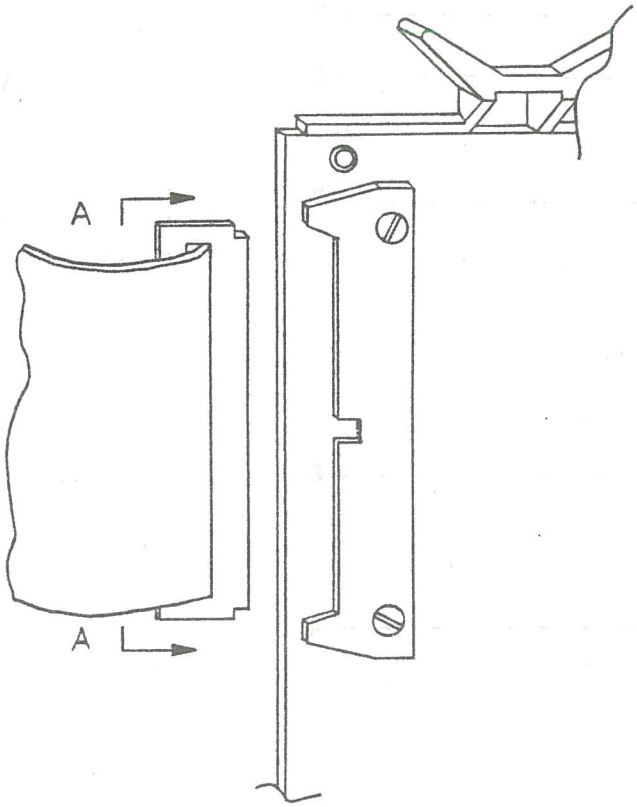


Figure 2-2
Connector Options Summary





FOR EIA

P2	NAME		P1	FUNCTION
2	TD	→	24	AFP-8S1
3	RD	←	23	AFP-8S0
4	RTS	→	29	EIA RTS
2Ø	DTR	→	33	EIA DTR
7	SG		40	EIA SIG GND

FOR TTY

SIGNAL		P1	P3
KEYBOARD CONTACTS	+	5	7
	−	8	3
PRINTER MAGNET	+	12	5
	−	16	2
READER RELAY CONTROL	−	14	4
	+	18	6

EIA Connection - The AFP-8 provides for EIA Received Data (RD) and EIA Transmitted Data (TD). It also asserts Data Terminal Ready (DTR) and Request To Send (RTS).

The following table summarizes the necessary connections for EIA operation.

Figure 2-3
EIA Operation

	J01 PIN NUMBER (AFP-8)	DB25S PIN NUMBER (DATA TERMINAL EQUIPMENT)
TD (TRANSMITTED DATA)	24	2
RD (RECEIVED DATA)	23	3
DTR (DATA TERMINAL READY)	33	20
RTS (REQUEST TO SEND)	29	4
SG (SIGNAL GROUND)	40	7

Options

The AFP-8 has provisions on the 40-pin cable header to permit configuration flexibility. All options discussed below, excluding power supply voltages, appear as simple 1.5Kohm pullup resisters to +5 volts. Electrically grounding any option pin on J01 enables that option or feature.

Baud Rate - Discrete baud rates from 50 to 9600 baud are selectable on J01. The following table (Fig. 2-4 on next page) represents all available baud rates and the appropriate programming pattern of J01 pins. The clock rate is a 16X clock.

Internal Clock - The internal clock is available at pin J01-38 and will be the baud rate selected by pins 25-28. The internal clock is capable of driving one standard TTL load.

External Clock - An external clock may be input to the AFP-8. Grounding pin J01-37 disables generation of the internal clock. The external clock is then input through pin J01-39. The external clock should be TTL compatible and have sufficient drive capability for one standard TTL load.

Local ECHO Suppression - If the local ECHO feature (produced for FPM functions) is to be inhibited, pin J01-7 is grounded. This does not in any way affect the AFP-8 in either mode of operation, but simply suppresses the echo of each input command to the local terminal.

FPM Disable - If the AFP-8 is to operate only in Teletype mode, pin J01-36 must be grounded. This prevents FPM operations.

Figure 2-4
Baud Rate Selection

J01
PIN NUMBER
(AFP-8)

28	27	26	25	BAUD RATE
				110
			X	150
		X		300
		X	X	2400
	X			1200
	X		X	1800
	X	X		4800
	X	X	X	9600
X				2400
X			X	600
X		X		200
X		X	X	134.5
X	X			75
X	X		X	50

X -- indicates pin is grounded

Switch Register LAS,OSR Disable - The AFP-8's SR operates in an inclusive "OR" relationship with the hardware Switch Register of a KC8 Programmer's Panel (if such is present on the PDP-8). If the user wishes to utilize the PDP-8 hardware switches, the AFP-8's SR can be disabled for the LAS and OSR instructions by grounding pin J01-22. This does not disable the AFP-8 SR for FPM functions. Alternately, setting the AFP-8's SR to 0000 will permit the KC8 Switch Register to operate normally.

IOT Device Codes - The Teletype mode of operation normally (with no additional programming) responds to IOT device codes 603X and 604X. Provision is made on pins 9, 10, and 11 on J01 to permit changing codes by appropriate pin programming.

Figure 2-5
IOT Device Code Selection

J01
PIN NUMBER
(AFP-8)

CODE	9	10	11
60*X			
61*X			X
62*X		X	
63*X		X	X
64*X	X		
65*X	X		X
66*X	X	X	
67*X	X	X	X

X -- indicates pin is grounded

* -- indicates octal 3 and 4

Power Supply Voltages - GND, +5 volts, -12 volts, and +12 volts are available on J01. The table on the next page shows where voltages are present on J01 and what amperage is available.

Figure 2-6
J01 Voltages

Pin J01	Voltage	Power
17	+5	1 amp
13	+12	250 ma
15	-12	250 ma

Ground: Pins 1,2,19,20,21,40

Restart - There are instances (such as a very large configuration with positive I/O options) when a hardware failure in the PDP-8 CPU can cause the HALT switch to be inoperative. This condition usually indicates the processor is "hung" in BUS NOT LAST XFER (TS3 timing state) Recovery by physically turning off the power supply and powering up is the only solution (unless the AFP-8 is installed).

The AFP-8 constantly samples TS3 to look for this occurance. If the AFP-8 sees a "hung" CPU in TS3 state for more than 100 msec, BUS POWER NOT OK is automatically asserted, bit "2000" of the readout sequence is set, and OMNIBUS signal POWER OK H is grounded. The CPU responds by falling into TS1 timing state with the machine halted. Recovery is effected through the AFP-8 by restarting the CPU in the normal manner.

Following is a short diagnostic to determine if the AFP-8 is operating properly. For this procedure, the AFP-8 is connected to a terminal and the AFP-8's baud rate is set at the terminal's rate. The CPU is assumed "on" and "halted". if a Programmers Panel (KC8) is installed, it is assumed to be in the following configuration: Switch Register switches 0:11 down; the Register Selector rotary switch in the "STATUS" position; and the "HALT", "SW",and "SS" switches up.

First, type a "B". This is a NOP command and should echo on the terminal simply as a "B".

The following short program is entered from the terminal to check for proper operation of the AFP-8. Carriage Returns and Line Feeds are typed after each DEP ("D" function):

```
0200FA
6031D
5200D
6034D
6046D
7200D
6041D
5205D
6042D
6003D
5253D
6035D
6003D
7410D
5254D
7201D
6035D
7200D
6003D
5255D
6035D
6007D
6040D
6003D
5256D
6035D
6003D
7410D
5257D
7201D
```

```
6035D
7200D
6003D
5260D
1377D
3010D
1410D
7510D
5245D
6046D
7200D
6041D
5250D
5243D
3262D
3263D
3264D
3265D
3266D
3267D
5241D
0261D
0262D
0263D
0264D
0265D
0266D
7777D
0377A
0261D
```

The memory should now be checked with successive "EM" commands to see that the program was loaded properly. When the program has been loaded properly, start the processor at 0200 (0200APCG), and then type a character. The character should be echoed at the terminal followed by "123456". If there is a problem with the AFP-8, the chain of numbers will stop before 6. The first character not printed explains the error:

1	No keyboard interrupts
2	The interrupt enable does not clear
3	The interrupt enable does not set
4	No printer interupts
5	The interrupt enable does not clear
6	The interrupt enable does not set

The program loops at 0245 upon completion of printing. To continue the test, return to FPM, halt the processor, and restart at 0200.

Upon successful completion of this test, normal use of the AFP-8 can be expected. However, if any part of this test does not respond as indicated in the text, please contact DCA for further information.

Warranty

Digital Communications Associates warrants the AFP-8 ASCII Front Panel to be free from defects for one (1) year after shipment. DCA will repair or replace any AFP-8 found defective (abusive treatment excluded) at no charge except actual shipping costs.

DCA will repair or replace an AFP-8 found defective (abusive treatment excepted) any time after expiration of the one (1) year warranty period for a charge of $50. per board plus actual shipping costs.

Any board so repaired or replaced and subsequently found defective (abusive treatment excepted) is eligible any time for repair or replacement for a charge of $50 per board plus actual shipping costs.

AFP-8 TECHNICAL SPECIFICATION SUMMARY

Size	Single Module (quad-size, extended length, single thickness)
Electrical Requirements	1.20a of +5V; 0.05a of -15V; 0 of +15V
Physical Requirements	1 OMNIBUS slot
Baud Rates	110 - 9600 (asynchronous) programmable by selecting pins 25, 26, 27, and 28 of J01
Terminal Compatibility	All ASCII (e.g., TTY, LA36, VT50, etc.)
PDP-8 Compatibility	All /e/f/m/a OMNIBUS machines
Connector	40-pin 3M-3417 connector (J01) similiar to DEC BERG
20ma Connection	Connect pins 3 and 4 of J01
EIA Connection	Connect pins 3 and 6 of J01
On-board Clock	Crystal controlled 16X; available off-board by selecting pin 38 of J01
Modes	FPM (disable by grounding pin 36 of J01) Teletype (always enabled)
Power available	+5V available off-board by selecting pin 17 of J01 Ground is available off-board by selecting pins 1, 2, 19, 20, 21, or 40 of J01 +12V available off-board by selecting pin 13 of J01 -12V available off-board by selecting pin 15 of J01
IOT Codes	603X, 604X - others programmable by selecting pins 9, 10, and 11 of J01
OMNIBUS Drive	Open-collector logic
On-board SR	Bits 0:11 - disable by grounding pin 22 of J01
ECHO	Enabled (full-duplex) - disable by grounding pin 7 of J01
External Clock Input	Inhibited - selectable by disabling internal clock (ground pin 37 of J01) and grounding pin 39 of J01 with TTL input

AFP-8 TECHNICAL SPECIFICATION SUMMARY
Summary of Operating Modes

Front Panel Mode Summary

Figure 4-1 shows a simplified block diagram of FPM of the AFP-8. Each incoming serial character from the terminal is deserialized by a UART (Universal Asynchronous Receiver Transmitter) and decoded as one of the following: NUMBERS, CPU CONTROL CHARACTERS, READOUT CONTROL, MISCELLANEOUS CONTROL, or ILLEGAL characters. All characters typed while in FPM are echoed directly by the UART. Numbers are loaded into the SR and stored sequentially from left-to-right.

FPM of the AFP-8 uses PROM's to decode the single character commands in order to select and enable the appropriate logic. The CPU input functions are ignored unless the CPU is halted. The functions "A", "F", and "D" load the contents of the SR onto the DATA BUS along with one of the BUS signals, e.g., MEM START, LA, or INIT.

The output commands load the selected data into a 12-bit buffer register and transmit the digits to the terminal with a carriage return and a line feed.

The control commands decode, select, and assert the necessary signals for the command.

Characters not used by FPM are ignored and simply echoed.

Teletype Mode Summary

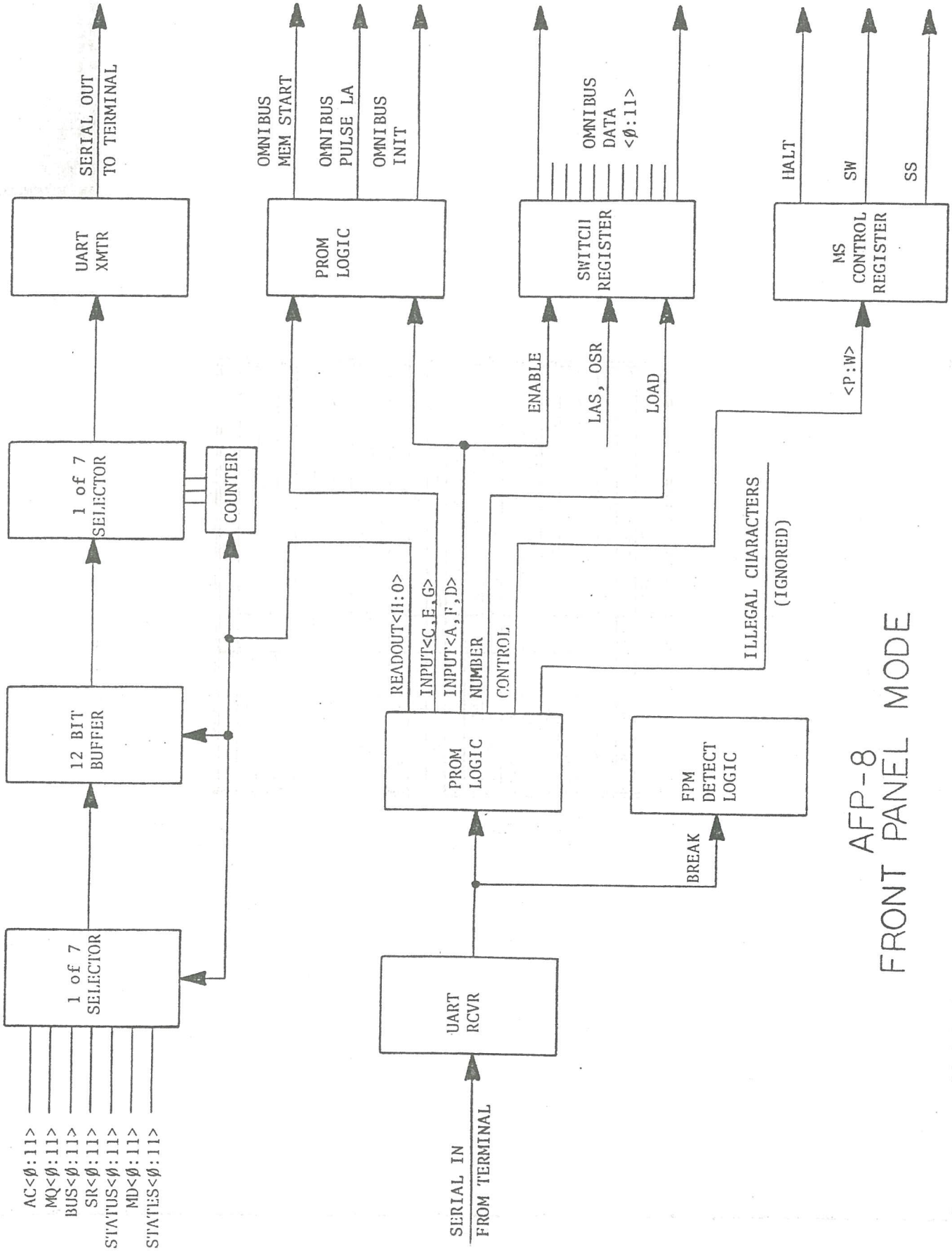
When the AFP-8 is not in FPM, it performs all functions of a Teletype control. Teletype mode of the AFP-8 converts parallel data words from the CPU to serial teletype characters. It converts serial Teletype characters into parallel data words for the computer.

The Teletype mode of the AFP-8 interprets two flags: the Teleprinter and Keyboard Flags. The transmitter section services the Keyboard while the receiver section services the Keyboard or Reader. Reader-Run is fully implemented on the AFP-8 to provide ASR paper tape control as does the KL8-XX.

PROM's are used to decode the Teletype IOT's.

For more detailed information on the operation of the logic of the AFP-8, please refer to the AFP-8 Drawing Set immediately following.

AFP-8 TECHNICAL SPECIFICATION SUMMARY
Front Panel Mode Summary



DRAWING LIST

DWG. NO.	NO.	TITLE
AFPV3 - CCI		COMPONENT INSTALLATION
AFPV3 - ISL		INTERRUPT & SKIP LOGIC
AFPV3 - REG		XMTR DATA MULTIPLEXER
AFPV3 - ROM		ROM DECODER
AFPV3 - SEL		TTY OR READOUT DATA SELECT
AFPV3 - SR		SWITCH & MASTER REGISTER
AFPV3 - TCL		TIMING CONTROL LOGIC
AFPV3 - UART		TRANSMITTER-RECEIVER UART
AFPV3 - TD1		TIMING DIAGRAM @→G
AFPV3 - TD2		TIMING DIAGRAM H→O
AFPV3 - TABLE 1		TRUTH TABLE FOR E12
AFPV3 - TABLE 2		TRUTH TABLE FOR E29
AFPV3 - TABLE 3		TRUTH TABLE FOR E41
AFPV3 - TABLE 4		TRUTH TABLE FOR E36
AFPV3 - MISC		MISCELLANEOUS
AFPV3 - LFC		LOGIC FLOW CHART

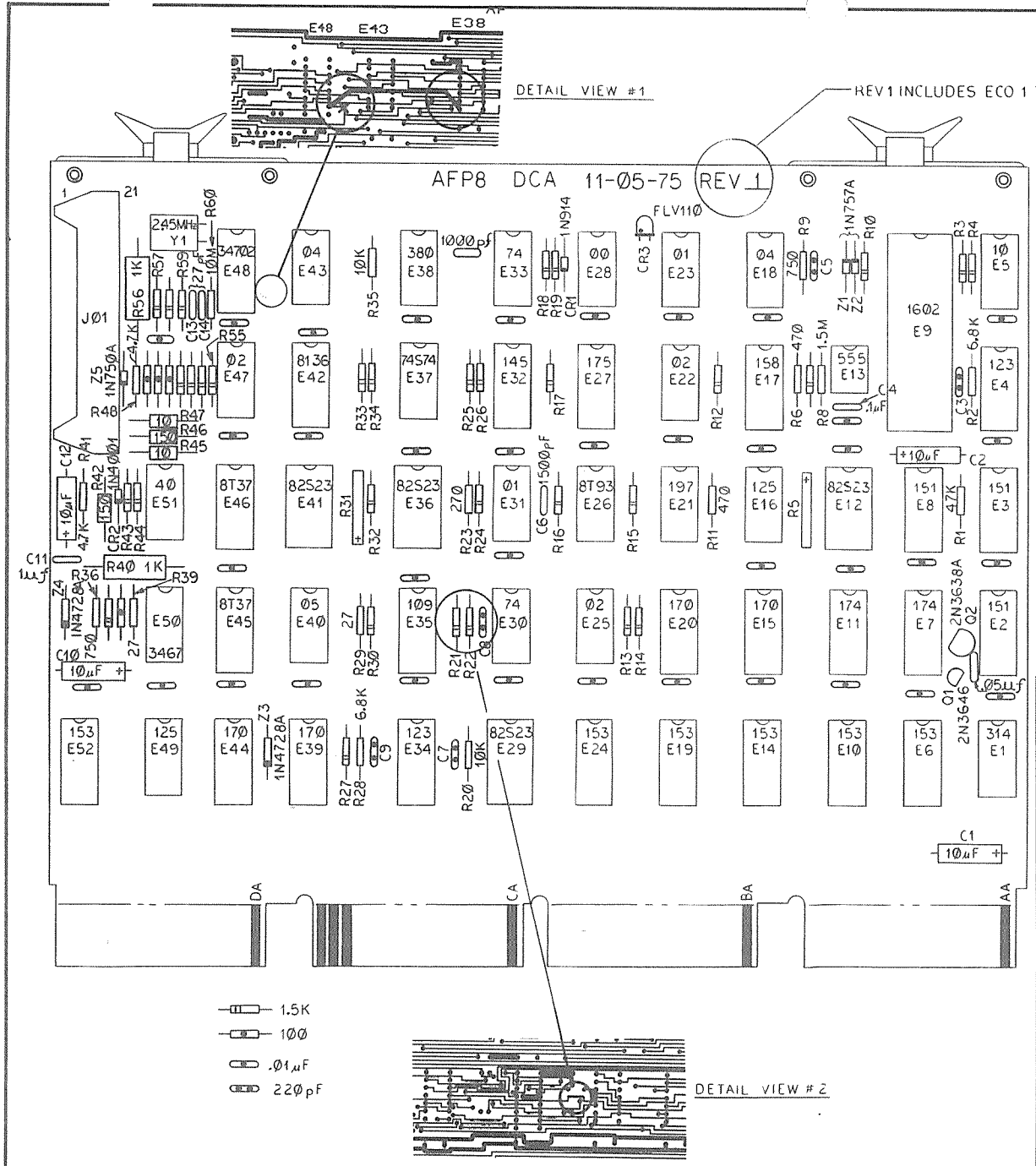
[redacted]

TITLE

ASCII FRONT PANEL

DATE	NUMBER	DRN EM
8 FEB 76	AFPV3-DL	CK

AFP-8 ASCII FRONT PANEL 1/3/77
Drawing Set



ECO LIST

1. ETCH CUT @ E48-10. E48-10 CONNECTED TO E38-7. (SEE DETAIL VIEW #1)
2. CONNECT TWO PIECES OF ETCH AS SHOWN IN DETAIL VIEW # 2.
3. REMOVE 1N914 ABOVE R5. CONNECT E13-07 TO LOWER VIA OF ABOVE MENTIONED 1N914.
4. ADD A .05μf CAPACITOR BETWEEN BASE OF Q2 AND GROUND.

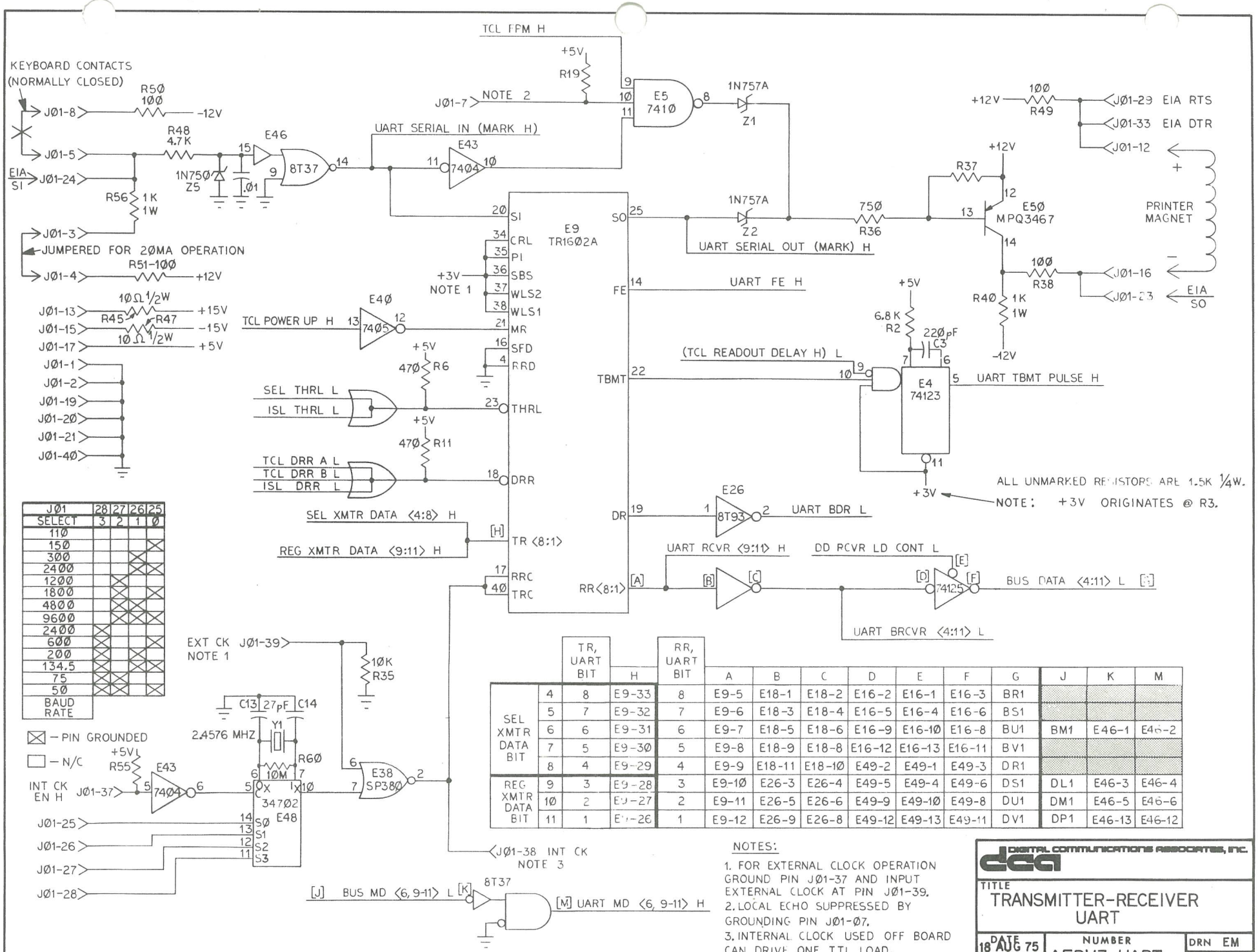
NO.	QTY.	DESCRIPTION
69	1	CAPACITOR .05μf
68	1	CAPACITOR 1μf
67	1	CAPACITOR 1000pf
66	1	FLV110 LED CR3
65	1	IC 74S74 E37
64	2	10Ω 1/2W R(45,47)
63	1	10M R60
62	1	1.5M R8
61	1	47K R1
60	2	1.5K SIP R(5,31)
59	2	10K R(20,35)
58	2	6.8K R(2,28)
57	2	4.7K R(41,48)
56	32	1.5K
55	2	1K, 1W R(40,56)
54	2	750Ω R(9,36)
53	2	470Ω R(6,11)
52	1	270Ω R23
51	2	150Ω, 1/2W R(42,46)
50	4	100Ω R(38,49,50,51)
49	2	27Ω R(29,39)
48	2	20 PIN IC STRIP
47	4	10μF C(1,2,10,12)
46	1	.1μF C4
45	1	1500pF C6
44	38	.01μF
43	2	27pF C(13,14)
42	5	220pF C(3,5,7,8,9)
41	1	2N3646 Q1
40	1	2N3638A Q2
39	1	IC 2N3467 E50
38	1	IC NE555 E13
37	1	IC SP314 E1
36	4	IC PROMS AV3E (12,29,36,41)
35	1	IC 8T93 E26
34	2	IC 8T37 E(45,46)
33	1	IC SP380 E38
32	1	IC DM8136 E42
31	1	IC TR1602 UART E9
30	1	IC 34702 E48
29	1	IC 74197 E21
28	1	IC 74175 E27
27	2	IC 74174 E(7,11)
26	4	IC 74170 E(15,20,39,44)
25	1	IC 74158 E17
24	6	IC 74153 E(6,10,14,19,24,52)
23	3	IC 74151 E(2,3,8)
22	1	IC 74145 E32
21	2	IC 74125 E(16,49)
20	2	IC 74123 E(4,34)
19	1	IC 74109 E35
18	2	IC 7474 E(30,33)
17	1	IC 7440 E51
16	1	IC 7410 E5
15	1	IC 7405 E40
14	2	IC 7404 E(18,43)
13	3	IC 7402 E(22,25,47)
12	2	IC 7401 E(23,31)
11	1	IC 7400 E28
10	2	1N4728A DIODES Z(3,4)
9	1	1N4001 DIODE CR2
8	1	1N914 DIODE CR1
7	1	1N750A DIODE Z5
6	2	1N757A DIODES Z(1,2)
5	1	3M HEADER 3432 J01
4	1	2.4576 MHZ CRYSTAL Y1
3	4	RIVETS
2	2	HANDLES
1	1	AFPV3 PC BOARD

PARTS LIST

DIGITAL COMMUNICATIONS ASSOCIATES, INC.

TITLE: COMPONENT INSTALLATION

DATE	NUMBER	DRN
5 FEB 76 22 NOV 76	AFPV3-CCI	EM CK



		TR, UART BIT	H	RR, UART BIT	A	B	C	D	E	F	G	J	K	M
SEL XMTR DATA BIT	4	8	E9-33	8	E9-5	E18-1	E18-2	E16-2	E16-1	E16-3	BR1			
	5	7	E9-32	7	E9-6	E18-3	E18-4	E16-5	E16-4	E16-6	BS1			
	6	6	E9-31	6	E9-7	E18-5	E18-6	E16-9	E16-10	E16-8	BU1	BM1	E46-1	E46-2
	7	5	E9-30	5	E9-8	E18-9	E18-8	E16-12	E16-13	E16-11	BV1			
	8	4	E9-29	4	E9-9	E18-11	E18-10	E49-2	E49-1	E49-3	DR1			
REG XMTR DATA BIT	9	3	E9-28	3	E9-10	E26-3	E26-4	E49-5	E49-4	E49-6	DS1	DL1	E46-3	E46-4
	10	2	E9-27	2	E9-11	E26-5	E26-6	E49-9	E49-10	E49-8	DU1	DM1	E46-5	E46-6
	11	1	E9-26	1	E9-12	E26-9	E26-8	E49-12	E49-13	E49-11	DV1	DP1	E46-13	E46-12

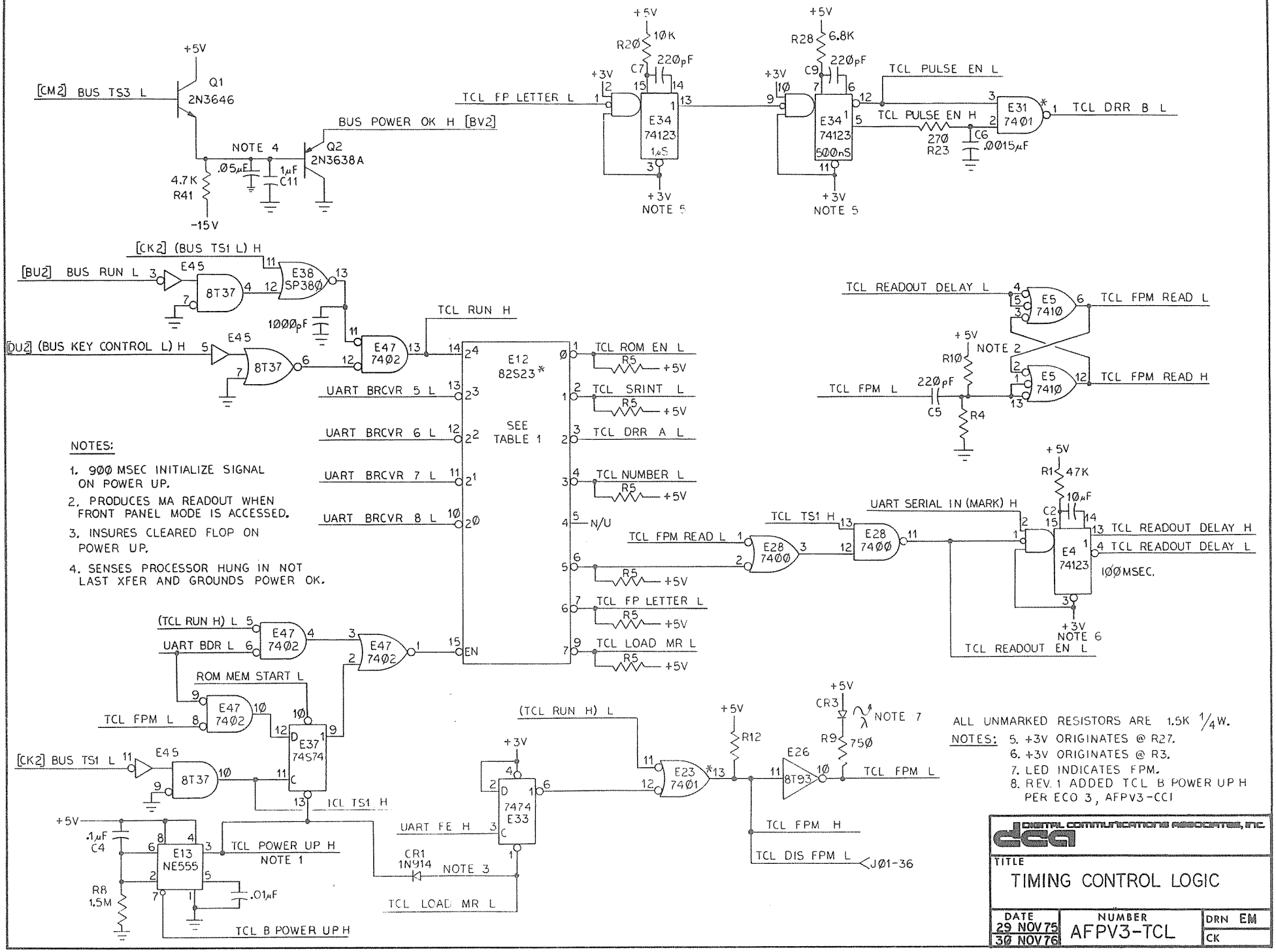
NOTES:

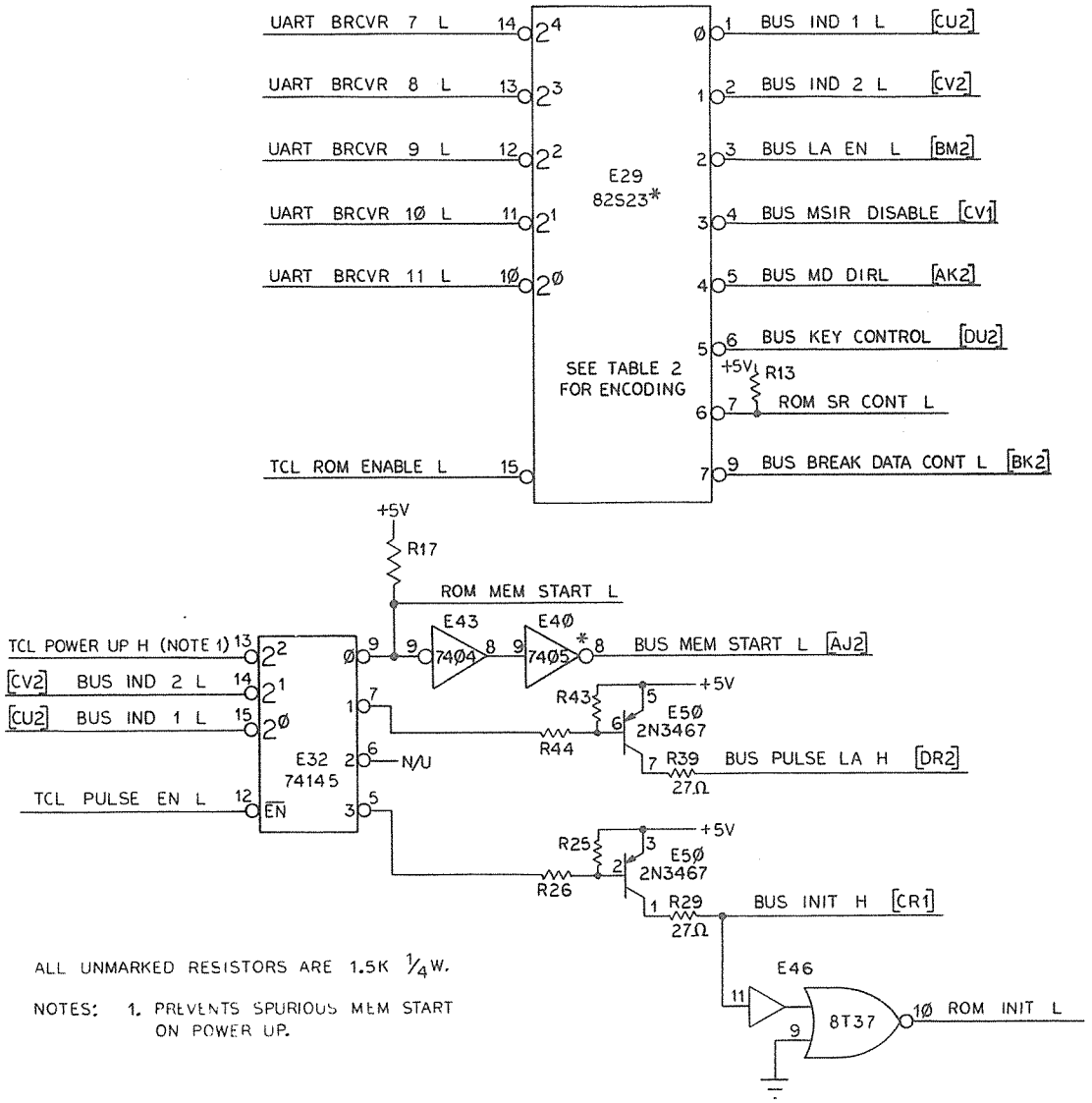
1. FOR EXTERNAL CLOCK OPERATION GROUND PIN JØ1-37 AND INPUT EXTERNAL CLOCK AT PIN JØ1-39.
2. LOCAL ECHO SUPPRESSED BY GROUNDING PIN JØ1-Ø7.
3. INTERNAL CLOCK USED OFF BOARD CAN DRIVE ONE TTL LOAD.

DIGITAL COMMUNICATIONS ASSOCIATES, INC.

TITLE
TRANSMITTER-RECEIVER UART

DATE	NUMBER	DRN EM
18 AUG 75 12 JAN 77	AFPV3-UART	CK

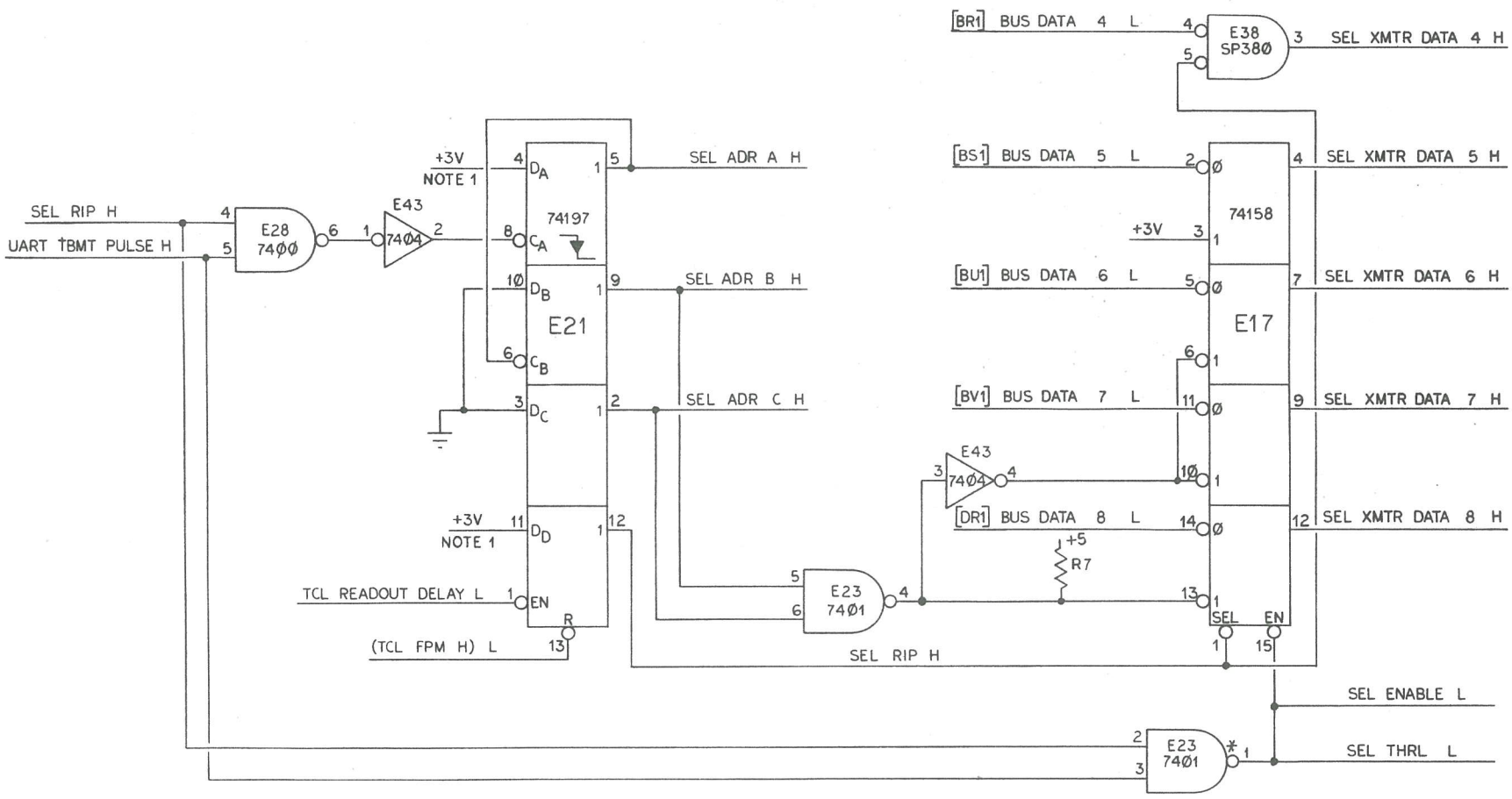

[CM2] BUS TS3 L
Q1
2N3646
+5V
NOTE 4
.05μF
1μF C11
4.7K R41
-15V
BUS POWER OK H [BV2]
Q2
2N3638A
TCL FP LETTER L
R20 10K
C7 220pF
+3V
E34 74123 1μS
+3V NOTE 5
R28 6.8K
C9 220pF
TCL PULSE EN L
TCL PULSE EN H
270 R23
C6 .0015μF
E31 7401
TCL DRR B L
[CK2] (BUS TS1 L) H
[BU2] BUS RUN L
E45 8T37
E38 SP380
1000pF
[DU2] (BUS KEY CONTROL L) H
E47 7402
TCL RUN H
E12 82S23*
SEE TABLE 1
UART BRCVR 5 L
UART BRCVR 6 L
UART BRCVR 7 L
UART BRCVR 8 L
TCL ROM EN L
TCL SRINT L
TCL DRR A L
TCL NUMBER L
N/U
TCL FP LETTER L
TCL LOAD MR L
R5 +5V
TCL READOUT DELAY L
E5 7410
TCL FPM READ L
TCL FPM READ H
NOTE 2
R10
220pF C5
R4
TCL FPM L
NOTES:
1. 900 MSEC INITIALIZE SIGNAL ON POWER UP.
2. PRODUCES MA READOUT WHEN FRONT PANEL MODE IS ACCESSED.
3. INSURES CLEARED FLOP ON POWER UP.
4. SENSES PROCESSOR HUNG IN NOT LAST XFER AND GROUNDS POWER OK.
UART SERIAL IN (MARK) H
R1 47K
10μF C2
TCL TS1 H
E28 7400
E4 74123
100MSEC.
TCL READOUT DELAY H
TCL READOUT DELAY L
TCL READOUT EN L
(TCL RUN H) L
UART BDR L
ROM MEM START L
E37 74S74
TCL TS1 H
E13 NE555
.1μF C4
R8 1.5M
.01μF
TCL POWER UP H
NOTE 1
TCL B POWER UP H
UART FE H
CR1 1N914
NOTE 3
E33 7474
E23 7401
R12
CR3
NOTE 7
R9 75Ø
E26 8T93
TCL FPM H
TCL DIS FPM L
J01-36
ALL UNMARKED RESISTORS ARE 1.5K 1/4W.
NOTES: 5. +3V ORIGINATES @ R27.
6. +3V ORIGINATES @ R3.
7. LED INDICATES FPM.
8. REV 1 ADDED TCL B POWER UP H PER ECO 3, AFPV3-CCI
DIGITAL COMMUNICATIONS ASSOCIATES, INC.
TITLE
TIMING CONTROL LOGIC
DATE 29 NOV 75 30 NOV 76
NUMBER AFPV3-TCL
DRN EM
CK



ALL UNMARKED RESISTORS ARE 1.5K 1/4W.

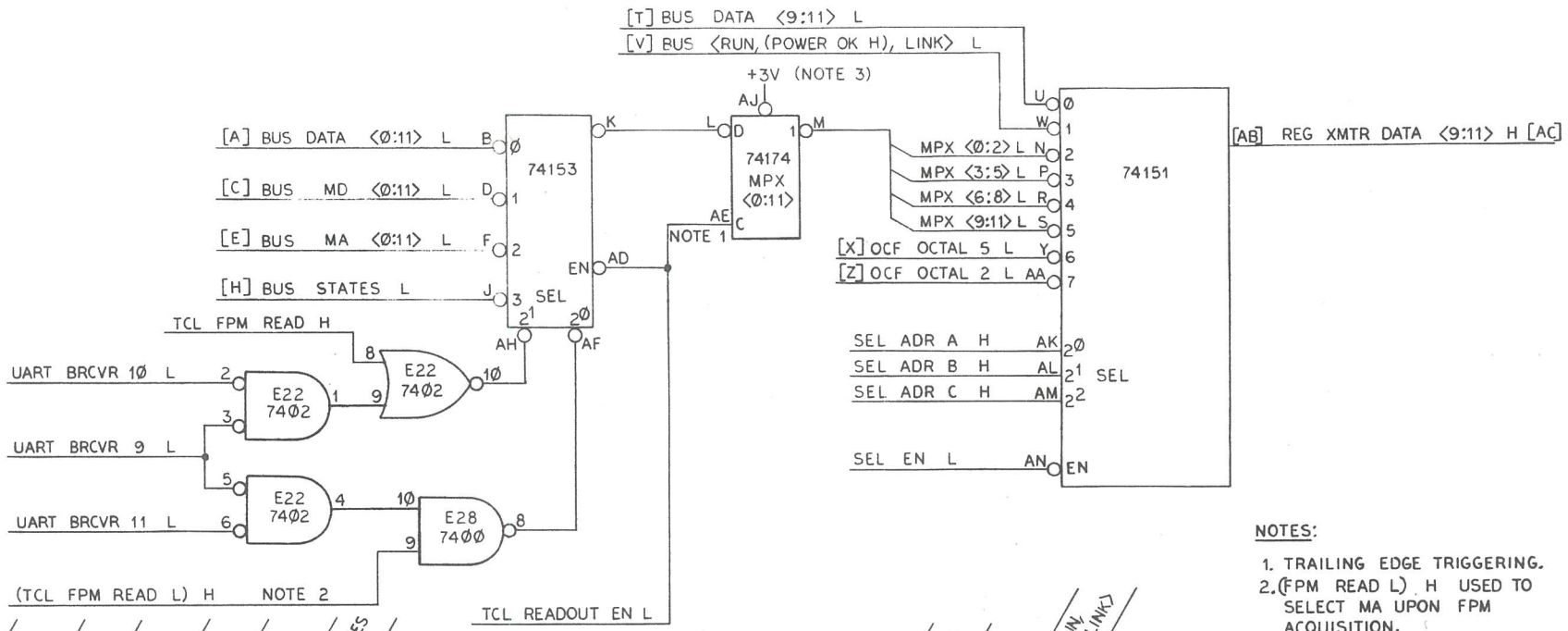
NOTES: 1. PREVENTS SPURIOUS MEM START ON POWER UP.

DIGITAL COMMUNICATIONS ASSOCIATES, INC.		
TITLE: ROM DECODER		
DATE: 30 JULY 75	NUMBER: AFPV3-ROM	DRN EM / CK BC



NOTES: 1. +3V ORIGINATES @ R15.

digital communications associates, inc.		
TITLE: TTY OR READOUT DATA SELECT		
DATE: 29JULY75	NUMBER: AFPV3-SEL	DRN EM CK BC



NOTES:

1. TRAILING EDGE TRIGGERING.
2. (FPM READ L) H USED TO SELECT MA UPON FPM ACQUISITION.
3. +3V GENERATED @ R3.

	BUS DATA		BUS MD		BUS MA		BUS STATES				MPX Ø:11	MPX Ø:2	MPX 3:5	MPX 6:8	MPX 9:11	BUS DATA		BUS (RUN, PWR OK, LINK)							
LINE	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	LINE
00	AR1	E06-03	AK1	E06-04	AD1	E06-05	DJ2	E06-06	E06-07	E07-14	E07-15	E08-02														00
01	AS1	E14-03	AL1	E14-04	AE1	E14-05	DK2	E14-06	E14-07	E07-04	E07-05	E02-02														01
02	AU1	E24-03	AM1	E24-04	AH1	E24-05	DL2	E24-06	E24-07	E11-11	E11-10	E03-02														02
03	AV1	E06-13	AP1	E06-12	AJ1	E06-11	DD2	E06-10	E06-09	E07-13	E07-12		E08-01													03
04	BR1	E14-13	BK1	E14-12	BD1	E14-11	DE2	E14-10	E14-09	E07-03	E07-02		E02-01													04
05	BS1	E24-13	BL1	E24-12	BE1	E24-11	DH2	E24-10	E24-09	E11-06	E11-07		E03-01													05
06	BU1	E10-03	BM1	E10-04	BH1	E10-05	AK2	E10-06	E10-07	E07-11	E07-10			E08-15												06
07	BV1	E19-03	BP1	E19-04	BJ1	E19-05	BK2	E19-06	E19-07	E11-14	E11-15			E02-15												07
08	DR1	E52-03	DK1	E52-04	DD1	E52-05	DV2	E52-06	E52-07	E11-04	E11-05			E03-15												08
09	DS1	E10-13	DL1	E10-12	DE1	E10-11	CD1	E10-10	E10-09	E07-06	E07-07				E08-14	DS1	E08-04	BU2	E08-03	GND	E08-13	+3	E08-12	E08-06	E09-28	09
10	DU1	E19-13	DM1	E19-12	DH1	E19-11	BE2	E19-10	E19-09	E11-13	E11-12				E02-14	DU1	E02-04	BV2	E02-03	+3	E02-13	GND	E02-12	E02-06	E09-27	10
11	DV1	E52-13	DP1	E52-12	DJ1	E52-11	BL2	E52-10	E52-09	E11-03	E11-02				E03-14	DV1	E03-04	AV2	E03-03	GND	E03-13	+3	E03-12	E03-06	E09-26	11

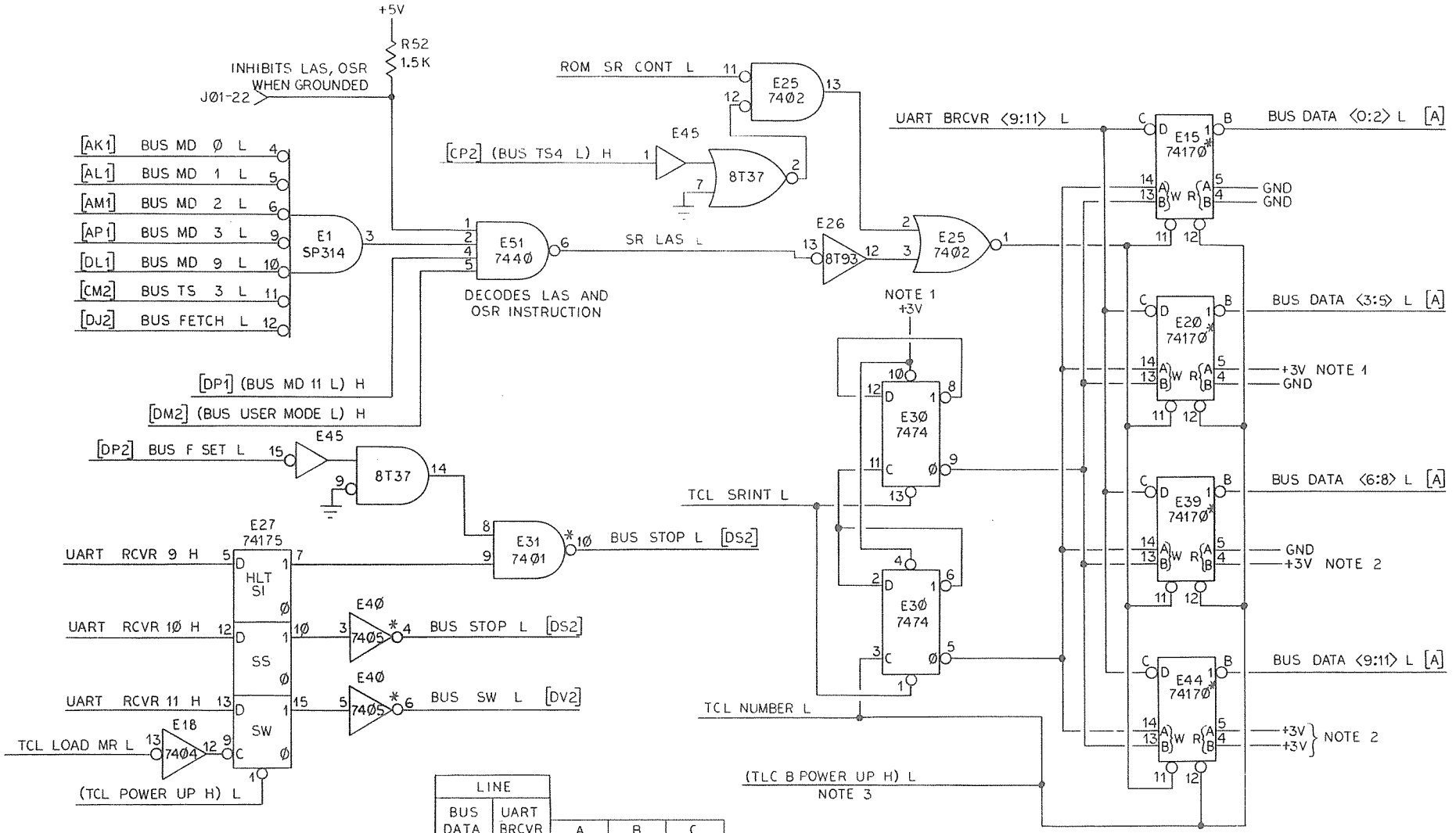
	TCL READOUT EN					SEL ADR A	SEL ADR B	SEL ADR C	SEL ENABLE	
LINE	AD	AE	AF	AH	AJ	AK	AL	AM	AN	LINE
00	E06-01	E07-09	E06-14	E06-02	E07-01					00
01	E14-01	E07-09	E14-14	E14-02	E07-01					01
02	E24-01	E11-09	E24-14	E24-02	E11-01					02
03	E06-15	E07-09	E06-14	E06-02	E07-01					03
04	E14-15	E07-09	E14-14	E14-02	E07-01					04
05	E24-15	E11-09	E24-14	E24-02	E11-01					05
06	E10-01	E07-09	E10-14	E10-02	E07-01					06
07	E19-01	E11-09	E19-14	E19-02	E11-01					07
08	E52-01	E11-09	E52-14	E52-02	E11-01					08
09	E10-15	E07-09	E10-14	E10-02	E07-01	E08-11	E08-10	E08-09	E08-07	09
10	E19-15	E11-09	E19-14	E19-02	E11-01	E02-11	E02-10	E02-09	E02-07	10
11	E52-15	E11-09	E52-14	E52-02	E11-01	E03-11	E03-10	E03-09	E03-07	11

DIGITAL COMMUNICATIONS ASSOCIATES, INC.

TITLE

XMTR DATA MULTIPLEXER

DATE	NUMBER	DRN EM
25 AUG 75	AFPV3-REG	CK



LINE				
BUS DATA	UART BRCVR	A	B	C
Ø	9	AR1	E15-9	E15-1
1	1Ø	AS1	E15-7	E15-2
2	11	AU1	E15-6	E15-3
3	9	AV1	E2Ø-9	E2Ø-1
4	1Ø	BR1	E2Ø-7	E2Ø-2
5	11	BS1	E2Ø-6	E2Ø-3
6	9	BU1	E39-9	E39-1
7	1Ø	BV1	E39-7	E39-2
8	11	DR1	E39-6	E39-3
9	9	DS1	E44-9	E44-1
1Ø	1Ø	DU1	E44-7	E44-2
11	11	DV1	E44-6	E44-3

NOTES:
1. +3V GENERATED @ R15.
2. +3V GENERATED @ R27.
3. POWER UP INITIALIZATION OF SR.
4. REV 1, ADD CONNECTION, TCL B POWER UP H TO TCL NUMBER L.

DIGITAL COMMUNICATIONS ASSOCIATES, INC.

TITLE: SWITCH & MASTER REGISTER

DATE	NUMBER	DRN
31 JULY 75 3Ø NOV 76	AFPV3-SR	EM CK BC

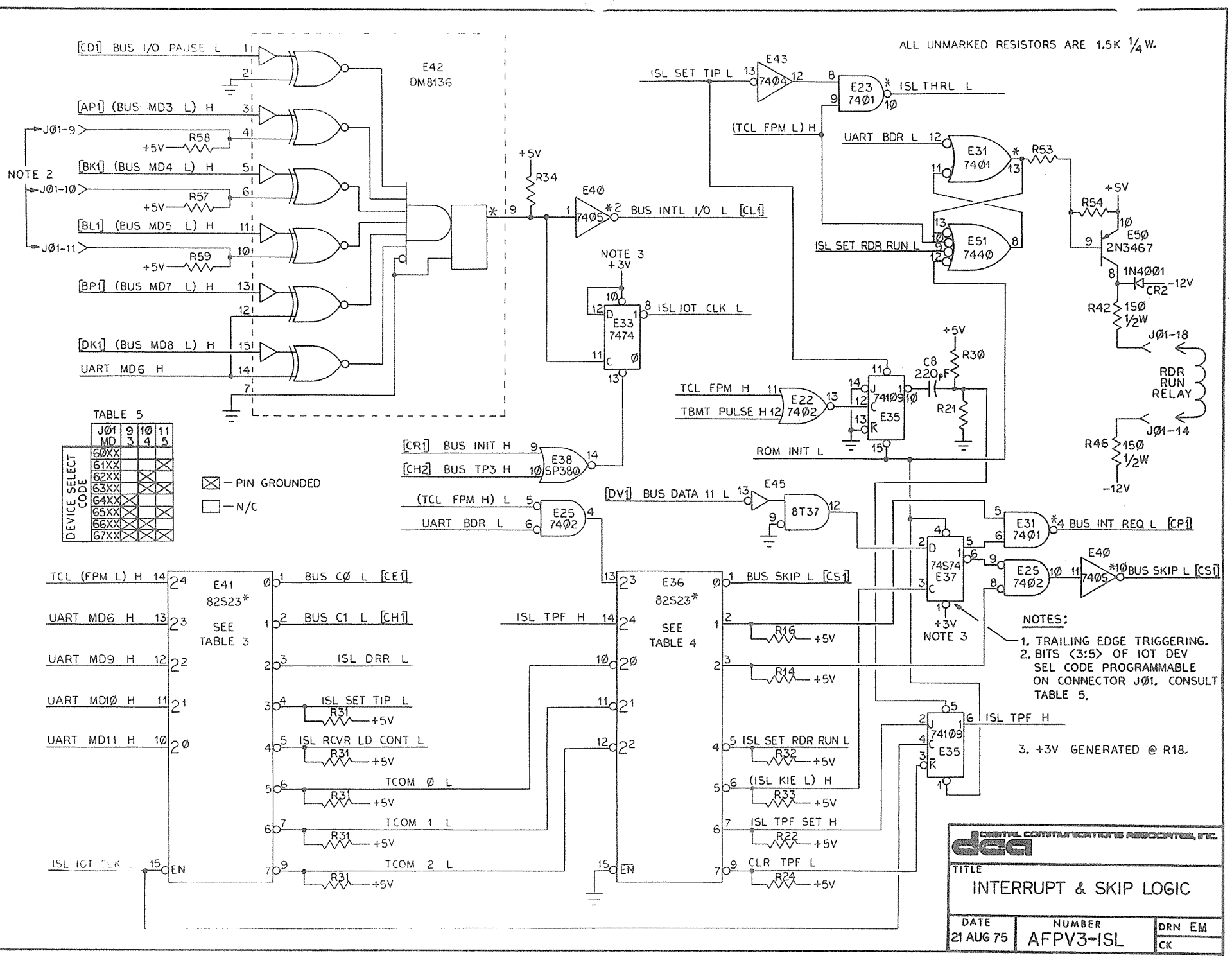

ALL UNMARKED RESISTORS ARE 1.5K 1/4 W.
E42
DM8136
[CD1] BUS I/O PAUSE L
[AP1] (BUS MD3 L) H
[BK1] (BUS MD4 L) H
[BL1] (BUS MD5 L) H
[BP1] (BUS MD7 L) H
[DK1] (BUS MD8 L) H
UART MD6 H
J01-9
J01-10
J01-11
NOTE 2
R58
R57
R59
+5V
R34
E40
7405
BUS INTL I/O L [CL1]
NOTE 3
+3V
E33
7474
ISL IOT CLK L
E43
7404
ISL SET TIP L
E23
7401
ISL THRL L
(TCL FPM L) H
UART BDR L
E31
7401
R53
R54
E50
2N3467
1N4001
CR2
-12V
R42
150
1/2W
J01-18
RDR
RUN
RELAY
J01-14
R46
ISL SET RDR RUN L
E51
7440
TCL FPM H
TBMT PULSE H
E22
7402
E35
74109
C8
220pF
R30
R21
ROM INIT L
[CR1] BUS INIT H
[CH2] BUS TP3 H
E38
SP380
(TCL FPM H) L
UART BDR L
E25
7402
[DV1] BUS DATA 11 L
E45
8T37
E31
7401
BUS INT REQ L [CP1]
E37
74S74
E40
7405
BUS SKIP L [CS1]
+3V
NOTE 3
TABLE 5
DEVICE SELECT CODE
JØ1 MD
9 3
10 4
11 5
60XX
61XX
62XX
63XX
64XX
65XX
66XX
67XX
PIN GROUNDED
N/C
E41
82S23*
SEE TABLE 3
TCL (FPM L) H
UART MD6 H
UART MD9 H
UART MD10 H
UART MD11 H
ISL IOT CLK
BUS CØ L [CE1]
BUS C1 L [CH1]
ISL DRR L
ISL SET TIP L
ISL RCVR LD CONT L
TCOM Ø L
TCOM 1 L
TCOM 2 L
R31
E36
82S23*
SEE TABLE 4
ISL TPF H
BUS SKIP L [CS1]
ISL SET RDR RUN L
(ISL KIE L) H
ISL TPF SET H
CLR TPF L
R16
R14
R32
R33
R22
R24
NOTES:
1. TRAILING EDGE TRIGGERING.
2. BITS <3:5> OF IOT DEV SEL CODE PROGRAMMABLE ON CONNECTOR JØ1. CONSULT TABLE 5.
3. +3V GENERATED @ R18.
DIGITAL COMMUNICATIONS ASSOCIATES, INC.
TITLE
INTERRUPT & SKIP LOGIC
DATE
21 AUG 75
NUMBER
AFPV3-ISL
DRN EM
CK

TABLE 1

FUNCTION	ADDRESS					BLAST FILE CODE	WORD BITS ⟨Ø:7⟩								8-BIT BLAST CODE	COMMENTS
	TCL RUN H	BRCVR 5 L	BRCVR 6 L	BRCVR 7 L	BRCVR 8 L		TCL MR LOAD L	TCL FP LETTER L	TCL READOUT EN L	NOT USED	TCL NUMBER L	TCL DRR L	TCL SRINT L	TCL ROM EN L		
	2^4	2^3	2^2	2^1	2^0		7	6	5	4	3	2	1	Ø		
x→DELETE	L	L	L	L	L	Ø						L	L		371	NOP
p→w					H	1	L					L	L		171	SAME AS P→W
h→o				H		2			L			L	L	L	33Ø	SAME AS H→O
\→g				H	H	3		L					L	L	274	SAME AS A→G
X→←			H			4						L	L		371	NOP
P→W			H		H	5	L					L	L		171	SW, SS, SI, HALT, CLR, CONTROL REG
H→O			H	H		6			L			L	L	L	33Ø	READOUT AC, MD, MA, MQ, DATA, STATES, STATUS
@, A→G			H	H	H	7		L					L	L	274	LD ADR, EXTD ADD, DEP, EXAM, CLR, CONT
8→?		H				1Ø						L	L		371	NOP
Ø→7		H			H	11					L	L			363	NUMBERS Ø→7
(→/		H		H		12						L	L		371	NOP
SPACE→'		H		H	H	13						L	L		371	NOP
↑X→CTRL SHFT O		H	H			14						L	L		371	NOP
↑P→↑W		H	H		H	15						L	L		371	NOP
↑H→↑O		H	H	H		16						L	L		371	NOP
NULL→↑G		H	H	H	H	17						L	L		371	NOP
↑	H					2Ø						L	L		371	NOP
	H				H	21	L					L	L		171	SAME AS P→W
	H			H		22			L			L	L	L	33Ø	SAME AS H→O
	H			H	H	23						L	L		371	PREVENTS A→G WHEN BUS RUN L
	H		H			24						L	L		371	NOP
SAME AS UPPER	H		H		H	25	L					L	L		171	SAME AS P→W
16 WORDS	H		H	H		26			L			L	L	L	33Ø	SAME AS H→O
EXCEPT WITH MACHINE	H		H	H	H	27						L	L		371	PREVENTS A→G WHEN BUS RUN L
RUNNING	H	H				3Ø						L	L		371	NOP
	H	H			H	31					L	L			363	NUMBERS Ø→7
	H	H		H		32						L	L		371	NOP
	H	H		H	H	33						L	L		371	NOP
	H	H	H			34						L	L		371	NOP
	H	H	H		H	35						L	L		371	NOP
	H	H	H	H		36						L	L		371	NOP
↓	H	H	H	H	H	37						L	L		371	NOP

NOTES:

1. THIS ROM IS THE PRINCIPAL SOURCE FOR TIMING AND CONTROL LOGIC.
2. ROM PART # AV3E12.

DIGITAL COMMUNICATIONS ASSOCIATES, INC.

TITLE: TRUTH TABLE FOR PROM @ E12

DATE	NUMBER	DRN EM
4 SEPT 75	AFPV3 – TABLE 1	CK

TABLE 2

FUNCTION	ADDRESS					BLAST FILE CODE	WORD BITS ⟨Ø:7⟩								8-BIT BLAST CODE	COMMENTS
	BRCVR 7 L	BRCVR 8 L	BRCVR 9 L	BRCVR 10 L	BRCVR 11 L		BUS BK DATA CONT L	ROM SR CONT L	BUS KEY CTL L	BUS MD DIR L	BUS MS IR DIS L	BUS LA EN L	BUS IND 2	BUS IND 1		
	2^4	2^3	2^2	2^1	2^0		7	6	5	4	3	2	1	Ø		
	L	L	L	L	L	Ø									377	
					H	1										
UPPER 16 WORDS				H		2										
ARE NEVER ENABLED				H	H	3										
ON THIS ROM			H			4										
			H		H	5										
			H	H		6										BARRING ANY
			H	H	H	7										INCORRECT ENABLE
W, w HALT, SS, SW		H				1Ø										SIGNALS, THESE CODES
V, v HALT, SS		H			H	11										ARE IRRELEVANT
U, u HALT, SW		H		H		12										
T, t HALT, SI		H		H	H	13										
S, s SET, SS, SW		H	H			14										
R, r SET, SS		H	H		H	15										
Q, q SET, SW		H	H	H		16										
P, p CLR CONTROL REG		H	H	H	H	17									377	
O, o STATES READ	H					2Ø							L	L	374	
N, n MA READ	H				H	21								L	376	
M, m MD READ	H			H		22							L		375	
L, l STATUS READ	H			H	H	23									377	
K, k SR READ	H		H			24		L					H	L	276	
J, j DATA READ	H		H		H	25								L	376	
I, i MQ READ	H		H	H		26							L		375	
H, h AC READ	H		H	H	H	27							L	L	374	
G, g CONTINUE	H	H				3Ø									377	
F, f LOAD EXTD ADR	H	H			H	31		L	L			L		L	232	
E, e EXAMINE	H	H		H		32	L		L	L	L				1Ø7	THESE FUNCTIONS
D, d DEPOSIT	H	H		H	H	33		L	L		L				227	ONLY WHEN MACHINE
C, c CLR AC, LINK	H	H	H			34							L	L	374	IS HALTED
B, b NOP	H	H	H		H	35							L		375	
A, a LOAD ADDRESS	H	H	H	H		36		L			L	L		L	262	
@, ` NOP	H	H	H	H	H	37							L		375	

NOTES:

1. ROM PART # AV3E29.

DIGITAL COMMUNICATIONS ASSOCIATES, INC.

TITLE: TRUTH TABLE FOR PROM @ E29

DATE	NUMBER	DRN EM
4 SEPT 75	AFPV3 – TABLE 2	CK

TABLE 3

FUNCTION	IOT	ADDRESS (TCL FPM L) H	MD6 H	MD9 H	MDIØ H	MD11 H	BLAST FILE CODE	WORD BITS ⟨Ø:7⟩ DD TCOM 2 L	DD TCOM 1 L	DD TCOM Ø L	DD RCVR LD CONT L	DD SET TIP L	DD DRR L	BUS C1 L	BUS CØ L	8-BIT BLAST CODE	COMMENTS
		2^4	2^3	2^2	2^1	2^0		7	6	5	4	3	2	1	Ø		
KCF	6Ø3Ø	L	L	L	L	L	Ø	H	H	H	H	H	H	H	H	377	KEYBOARD IOT
KSF	6Ø31					H	1									377	SERVICE IGNORED
KCC	6Ø32				H		2									377	WHEN IN FPM TO
NOT USED	N/U				H	H	3									377	AVOID INTERFERENCE KBD
KRS	6Ø34			H			4									377	WITH FPM
KIE	6Ø35			H		H	5									377	FUNCTIONS
KRB	6Ø36			H	H		6									377	
NOT USED	N/U			H	H	H	7									377	FPM
TFL	6Ø4Ø		H				1Ø	L	L							Ø77	
TSF	6Ø41		H			H	11		L							277	
TCF	6Ø42		H		H		12	L	L	L						Ø37	
NOT USED	N/U		H		H	H	13									377	TELETYPE TELEPRINTER
TPC	6Ø44		H	H			14					L				367	SETS TPF WHEN IN FPM (DOES NOT PRINT)
TSK	6Ø45		H	H		H	15		L	L						237	
TLS	6Ø46		H	H	H		16	L	L	L		L				Ø27	SETS TPF WHEN IN FPM (DOES NOT PRINT)
TLSC	6Ø47		H	H	H	H	17	L	L	L		L			L	Ø26	SETS TPF, BUT DOES NOT PRINT WHEN IN FPM
KCF, CLEAR KBD FLAG	6Ø3Ø	H					2Ø						L			373	
KSF, SKP ON KBD FLAG	6Ø31	H				H	21			L						337	
KCC, CLR KBD FLAG & AC, ADVANCE RDR	6Ø32	H			H		22	L					L		L	172	
NOT USED	N/U	H			H	H	23									377	KBD
KRS, READ KBD BUFFER STATIC	6Ø34	H		H			24				L			L		355	
KIE, SET/CLEAR INT ENABLE	6Ø35	H		H		H	25	L		L						137	
KRB, READ KBD/ CLEAR FLAG	6Ø36	H		H	H		26	L			L		L	L	L	15Ø	
NOT USED	N/U	H		H	H	H	27									377	FPM
TFL, SET TPF	6Ø4Ø	H	H				3Ø	L	L							Ø77	
TSF, SKP ON TPF	6Ø41	H	H			H	31		L							277	
TCF, CLEAR TPF	6Ø42	H	H		H		32	L	L	L						Ø37	
NOT USED	N/U	H	H		H	H	33									377	TELETYPE TELEPRINTER
TPC, LOAD TP & PRINT	6Ø44	H	H	H			34					L				367	
TSK, SKP ON TPF OR KBD FLAG	6Ø45	H	H	H		H	35		L	L						237	
TLS, LOAD TP SEQUENCE	6Ø46	H	H	H	H		36	L	L	L		L				Ø27	
TLSC, TLS & CLA	6Ø47	H	H	H	H	H	37	L	L	L		L			L	Ø26	

NOTES:

1. ROM PART # AV3E41

DIGITAL COMMUNICATIONS ASSOCIATES, INC.

TITLE
TRUTH TABLE FOR PROM @ E41

DATE	NUMBER	DRN EM
2 SEPT 75	AFPV3–TABLE 3	CK

TABLE 4

FUNCTION	ADDRESS					BLAST FILE CODE	WORD BITS ⟨Ø:7⟩								8-BIT BLAST CODE	COMMENTS
	TPF H	DR FPM H ②	TCOM 2 L	TCOM 1 L	TCOM Ø L		CLEAR TPF L	SET TPF H	KIE L	SET RDR RUN L	NOT USED	INT ENABLE/ SKIP L	INT REQ H	BUS SKIP L		
	2^4	2^3	2^2	2^1	$2^Ø$		7	6	5	4	3	2	1	Ø		
CLEAR TP FLAG						Ø	L	L					L		Ø75	(TCF+TPC) · $\overline{TPF}$ · $\overline{KBF}$
SET TP FLAG					H	1							L		375	TFL · $\overline{TPF}$ · $\overline{KBF}$
KBD INT ENABLE				H		2		L	L				L		235	KIE · $\overline{TPF}$ · $\overline{KBF}$
SET RDR RUN RELAY				H	H	3		L		L			L		255	KCC · $\overline{TPF}$ · $\overline{KBF}$
NOP			H			4		L					L		275	TSK · $\overline{TPF}$ · $\overline{KBF}$
NOP			H		H	5		L					L		275	TSF · $\overline{TPF}$ · $\overline{KBF}$
NOP			H	H		6		L					L		275	KSF · $\overline{TPF}$ · $\overline{KBF}$
NOP			H	H	H	7		L					L		275	
CLEAR TP FLAG		H				1Ø	L	L							Ø77	(TCF+TPC) · $\overline{TPF}$ · KBF
SET TP FLAG		H			H	11									377	TFL · $\overline{TPF}$ · KBF
KBD INT EN		H		H		12		L	L						237	KIE · $\overline{TPF}$ · KBF
SET RDR RUN RELAY		H		H	H	13		L		L					257	KCC · $\overline{TPF}$ · KBF
SKP ON TP OR KB FLAG		H	H			14		L				L			273	TSK · $\overline{TPF}$ · KBF
NOP		H	H		H	15		L							277	TSF · $\overline{TPF}$ · KBF
SKP ON KBD FLAG		H	H	H		16		L						L	276	KSF · $\overline{TPF}$ · KBF
NOP		H	H	H	H	17		L							277	
CLEAR TP FLAG	H					2Ø	L	L							Ø77	(TCF+TPC) · TPF · $\overline{KBF}$
SET TP FLAG	H				H	21									377	TFL · TPF · $\overline{KBF}$
KBD INT ENABLE	H			H		22		L	L						237	KIE · TPF · $\overline{KBF}$
SET RDR RUN RELAY	H			H	H	23		L		L					257	KCC · TPF · $\overline{KBF}$
SKP ON TP OR KB FLAG	H		H			24		L				L			273	TSK · TPF · $\overline{KBF}$
SKP ON TPF	H		H		H	25		L						L	276	TSF · TPF · $\overline{KBF}$
NOP	H		H	H		26		L							277	KSF · TPF · $\overline{KBF}$
NOP	H		H	H	H	27		L							277	
CLEAR TP FLAG	H	H				3Ø	L	L							Ø77	(TCF+TPC) · TPF · KBF
SET TP FLAG	H	H			H	31									377	TFL · TPF · KBF
KBD INTERRUPT ENABLE	H	H		H		32		L	L						237	KIE · TPF · KBF
SET RDR RUN RELAY	H	H		H	H	33		L		L					257	KCC · TPF · KBF
SKP ON TP OR KB FLAG	H	H	H			34		L				L			273	TSK · TPF · KBF
SKP ON TELEPRINTER FLAG	H	H	H		H	35		L						L	276	TSF · TPF · KBF
SKP ON KBD FLAG	H	H	H	H		36		L						L	276	KSF · TPF · KBF
NOP	H	H	H	H	H	37		L							277	

NOTE 3

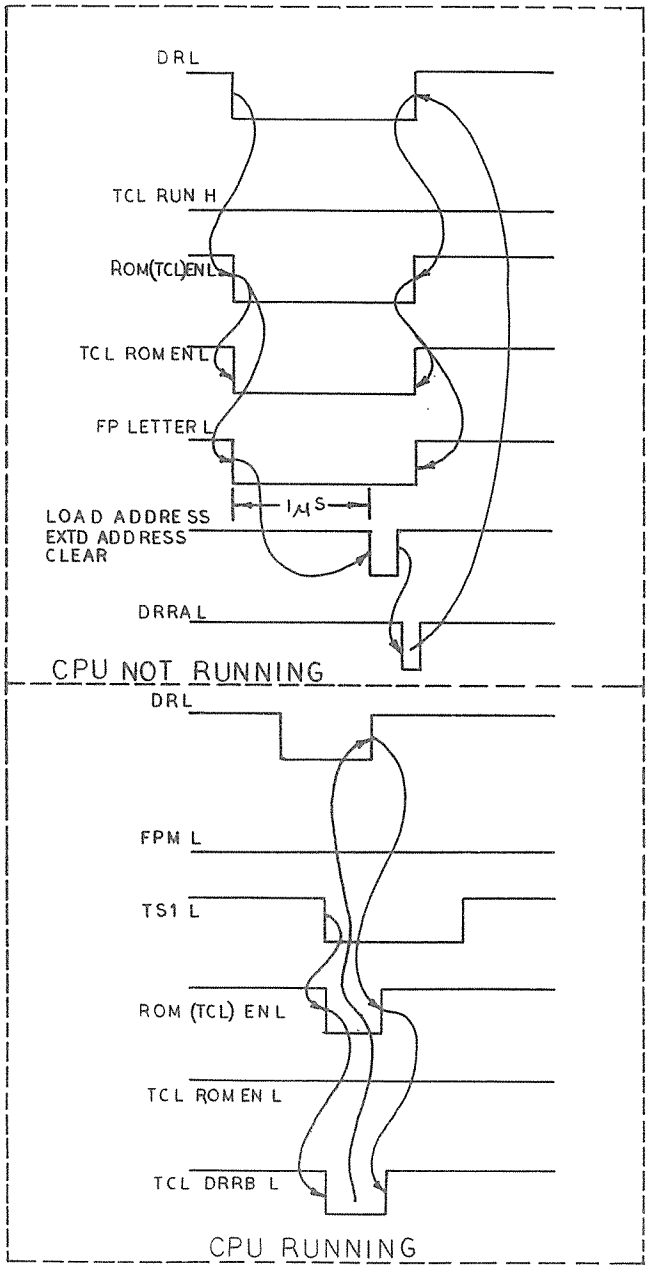
NOTES:

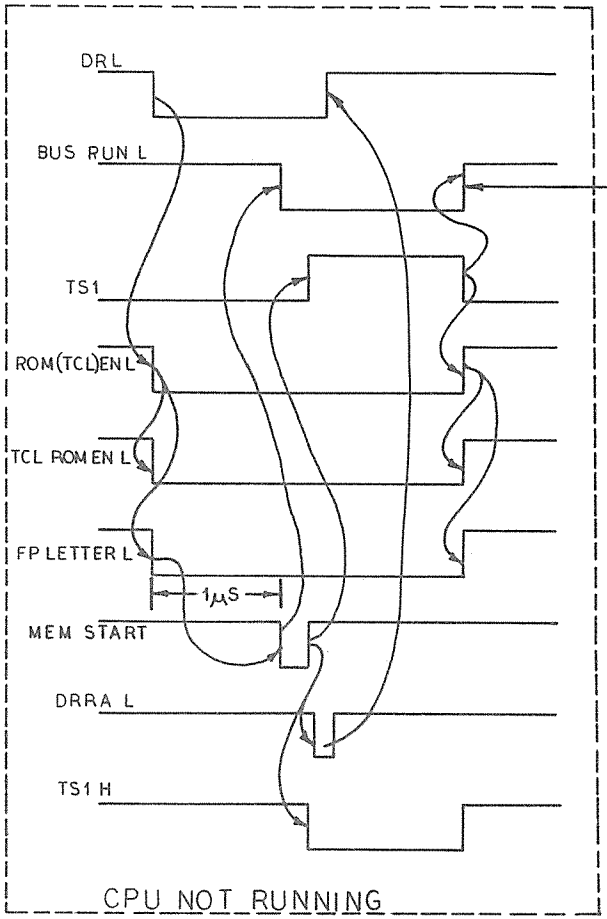
1. ROM PART # AV3E36.
2. DR FPM ASSERTED WHEN $\overline{FPM}$ AND DA.
3. REV 1, WORD 22 CHANGED FROM 267 TO 237.

DIGITAL COMMUNICATIONS ASSOCIATES, INC.

TITLE
TRUTH TABLE FOR PROM @ E36

DATE	NUMBER	DRN EM
3 SEPT 75 3Ø NOV 76	AFPV3-TABLE 4	CK



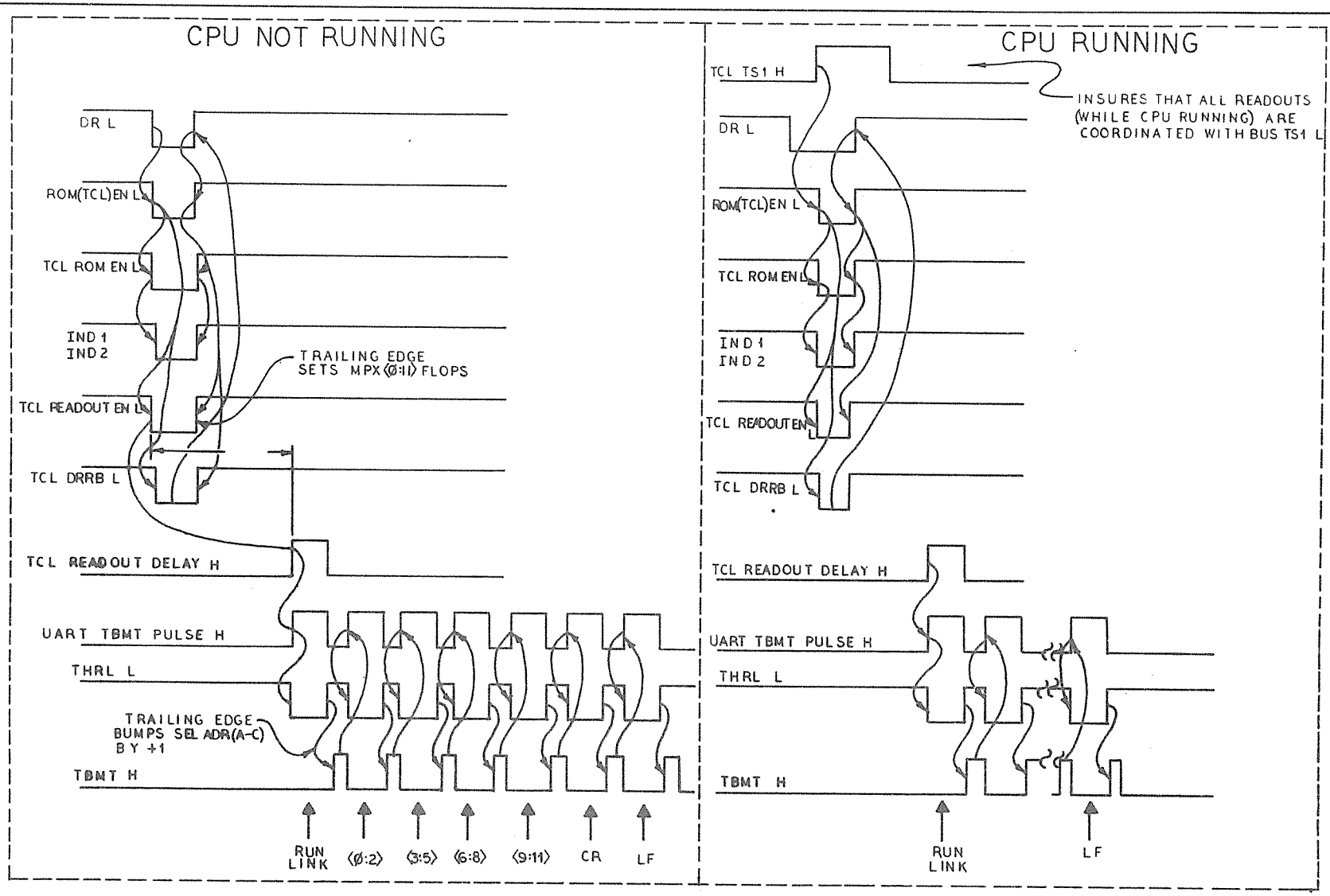


STOP IS ASSERTED BY TCL ROM EN L SO THAT RUN L ONLY STAYS UP UNTIL THE NEXT TS1↓ TRANSACTION.

THESE THREE TIMING DIAGRAMS ARE FOR THE LETTERS @ –G

@	NOT USED
A	LOAD ADDRESS
B	NOT USED
C	CLEAR
D	DEPOSIT
E	EXAMINE
F	LD EXTD ADDRESS
G	CONTINUE

TITLE: TIMING DIAGRAM @ –G		
DATE: 2-5-75	NUMBER: AFP-TD1	DRN RB CK

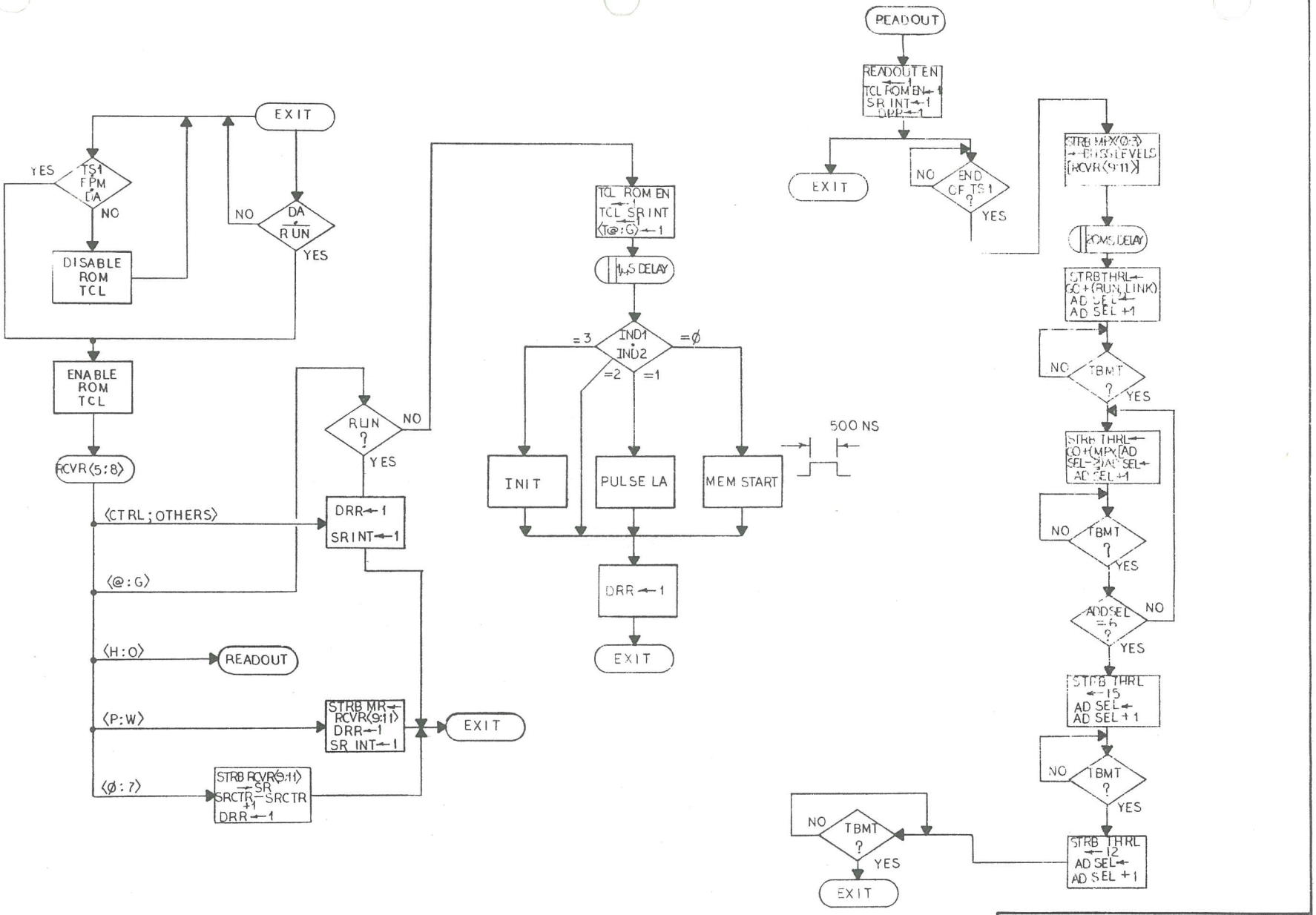


READOUTS (H→O)

H,K	AC READ
I	MQ READ
J	DATA READ
L	STATUS READ
M	MD READ
N	MA READ
O	STATES READ

TITLE
TIMING DIAGRAM H-O

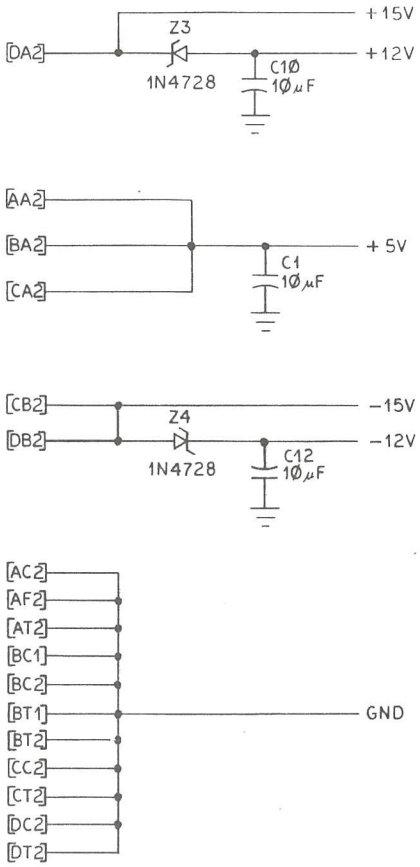
DATE	NUMBER	REV
2-5-75	AFP-TD2	

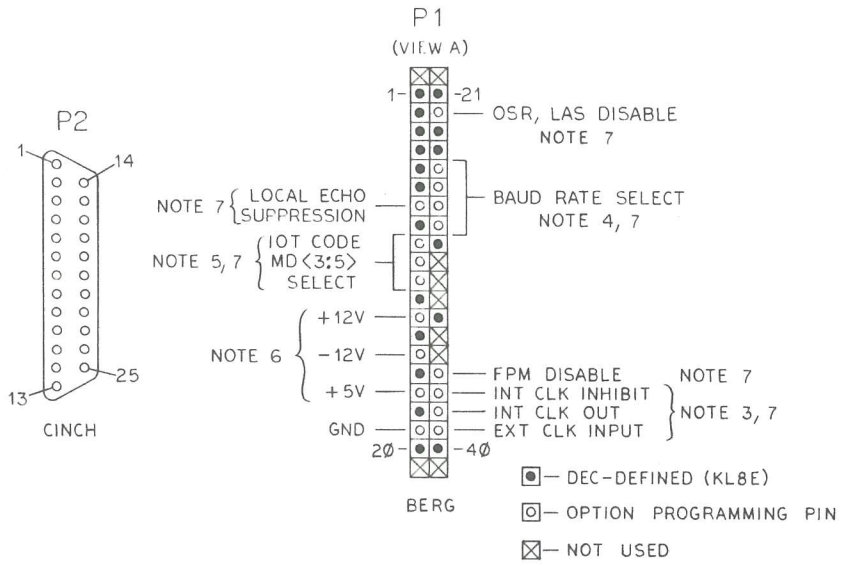


DIGITAL COMMUNICATIONS ASSOCIATES, INC.

TITLE
LOGIC FLOW CHART

DATE	NUMBER	DRN RB
1-20-75	AFPV3-LFC	CK





FOR EIA

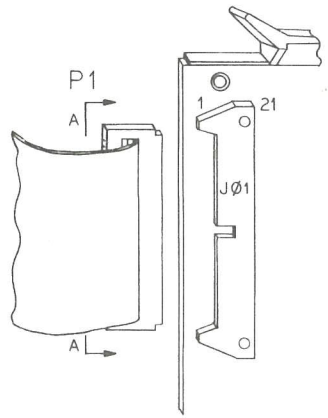
NOTE 1

TEPMINALS				MODEMS		
FUNTION	P2		P1		P2	FUNTION
SI	2	→	24	←	3	SO
SO	3	←	23	→	2	SI
CTS	5	←	29	←	4	RTS
DSR	6	←	33	←	20	DTR
SIG GND	7		40		7	SIG GND

FOR TTY

NOTE 2

SIGNAL		P1	P3
KEYBOARD CONTACTS	+	5	7
	–	8	3
PRINTER MAGNET	+	12	5
	–	16	2
READER RELAY CONTROL	–	14	4
	+	18	6



NOTES:

1. PINS 3 & 6 ON BERG CONNECTOR (P1) ARE CONNECTED VIA JUMPER FOR EIA APPLICATION.
2. PINS 1, 2, 21, & 40 OF P1 ARE ALL CONNECTED TO GROUND. PINS 3 & 4 ARE CONNECTED VIA JUMPER FOR 20 MA OPERATION.
3. THE INTERNAL CLOCK IS AVAILABLE TO DRIVE ONE TTL LOAD OFFBOARD @ JØ1-38. THE USE OF AN EXTERNAL CLOCK IS FACILITATED BY INHIBITING INTERNAL CLOCK (@ JØ1-37) AND INPUTTING EXTERNAL CLOCK @ JØ1-39.
4. SEE DRAWING AFPV3-UART FOR BAUD RATE SELECT PATTERN.
5. SEE DRAWING AFPV3-ISL FOR IOT DEVICE SELECT CODE OPTIONS.
6. ±12 VOLTS AVAILABLE AT 100 MA. +5 VOLTS AVAILABLE AT 1 AMP.
7. ALL PROGRAMMING OF OPTIONS IS ACCOMPLISHED BY GROUNDING THE RESPECTIVE OPTION PIN. GROUND IS AVAILABLE AS REFERRED TO IN NOTE 2.
8. REV 1, CHANGED TABLE FOR EIA

NOTE 8

DIGITAL COMMUNICATIONS ASSOCIATES, INC.

TITLE: MISCELLANEOUS: CABLE ASSY, CONNECTOR OPTIONS, OMNIBUS PWR CONN.

DATE	NUMBER	DRN EM
25 SEPT 75 30 NOV 76	AFPV3-MISC	CK

NOTES